

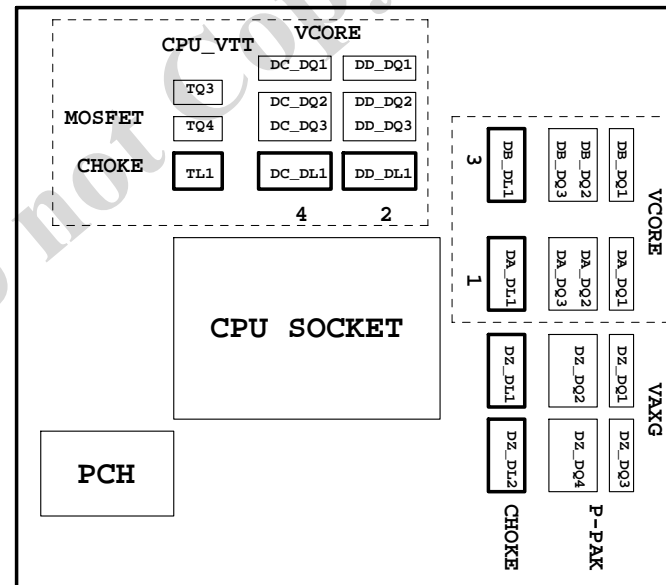
Model Name: GA-Z77-D3H

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*3 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	VT2021 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564
24	VCORE PWM DRIVER IR3598
25	NCP3933 OVER VOLTAGE
26	DISCRETE POWER
27	DDR_15V & CPU_VTT PWM IR3570

SHEET TITLE

28	DDR_15V & CPU_VTT PWM DRIVER CHL8550
29	VCCSA POWER
30	F_PANEL , F_USB2.0/3.0
31	ATX POWER, CLOCK GEN
32	HWM , KB/MS , FAN CTRL
33	LAN ATHEROS AR8151
34	N/A
35	M-SATA
36	DVI
37	HDMI , R_USB30
38	TABLE LIST
39	
40	



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Cover Sheet			
Title	GA-Z77-D3H		
Size	Document Number	Rev	1.1
Custom			
Date:	Friday, July 13, 2012	Sheet	1 of 38

GA-Z77-D3H

Component value change history

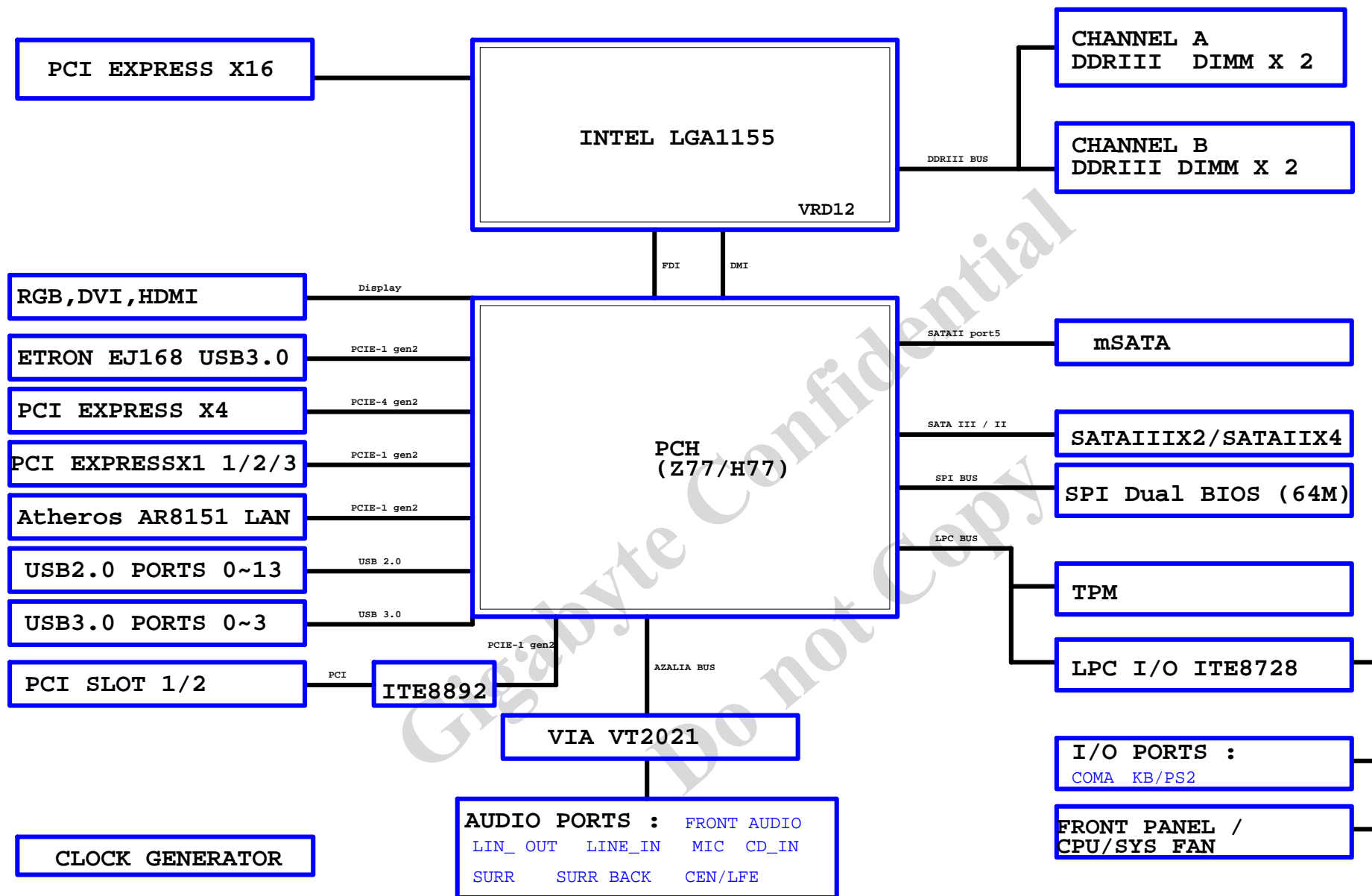
Data	Change Item	Reason
0.1-1124	E-BOM	
02-1216	1. ADD PCH_HS & MOS_HS料號	
	2. PCIE gen2 switch PI3PCIE2415ZHE --> ASM1440	
	3. load-line DAR5=12K , DAR40=1.78K	
10A-0105	1. Z77料號更新	
	2. PWM Driver power vcc or +12V?	
	3. DART2 --> 47K/1/4/S , DAR44 --> 0 ohm	
10B-0113	1. Vcore & VAXG VSEN modify , DAR1,DAR51=100/4/1,DAR2,DAR54=0/4,DAC1,DAC24=3.3nF	
	2. 1.54K加替料:10RC4-001541-22R TA-I	
	1. Remove IR PWM 1X3 pin	
10C-0117	1. DA_DR11,DC_DR11,DZ_DR18 1ohm --> 0ohm	
10D-0119	1. Prochot R65 : 1.65K/4/1 --> 2.74K/4/1	
10E-EVT-0201	1. Modify choke=0.36uH , DRIVER=5V	
10F	1. IR3564要改用新料號03R	
	2. poochot change 100K	
10T	1. 0 OHM Short-pad	
	2. DDR3 FOR OC 2400MHz UP	
10G-1.01	0. PCB Rev1.0 --> ReV1.01 (DDR3 OC 2400MHz+)	
	1. RS_PWM相關線路移除 (若有上prochot pull up改100 ohm)	
	2. Add M/B ID for DDR3 OC	
	3. 固態電容區分100uF/6.3V & 100uF/16V	
10H-1.02	1. PCB Rev1.01 --> ReV1.02 (DDR3 OC 2800MHz+)	
	2. Add M/B ID for DDR3 OC	
	3. ADD DC79 FOR A_CPUPWROK	
	4. 100u 16V-->6.3V	
10I-0430	1. PWM IR3564 --> IR3564A	
	2. Remove DAESD1	
	3. RJK0393DPA 10IF9-040393-01R --> 10IF9-040393-11R	

Circuit or PCB layout change

DATE	Change Item	Reason
P67X-UD3-B3		
2011/02/18-0.1	1. 移除LAR11 ,LAR14 , NR28 ,新增NTP11	
2011/02/18-1.0	2. 新增DR388,DR389,DR391 ; Remove DQ49,DR347,DR371 3. CR44改成R0603-RH 4. R1,LAR3,RBR20,LABC25 -->R0402-2-SHORT 5. RAQ1 --> Q_TO223-MASK 6. RARN1 --> R8P4R-0402-SHORT 7. CESD1-5 --> SSOP5 8. RAQ2,RAEC1一起往下移40mil 9. CESD2文字面要標pin1	
2011/03/8-1.01	1. Add "Dolby" logo	
2011/03/8-1.02	1. UAFB1,UAFB2,UBF1,UBF2 Footprint update 1206-->1812 2. Add "AD1" FOR 5VSB	
Z68XP-D3		
1.0	1. update MINI_PCIE footprint 2. 文字面 : SLOT部分全對齊	
Z77-D3H-0.1	EVT	
0.2-1216	1. Remove SE9172 , Add VCC3 內層(注意其他內層power,跨切割) 2. SPDIF AGND --> GND 3. PCI SLOT & PCIEX1/X4 CAP COST DOWN 4. 0 ohm --> SHORT PAD 5. REMOVE SMBUS FROM COMP TO SOLDER SIDE IN DR POWER 6. SATA3 connect Change to 90 degree (記得SATA3訊號部分要做挖空) 7. Add "108dB"文字面 8. Remove VCC1_05_PCH & VCC1_8_PCH gate net 9. Add EJ168 R_USB30_1 & F_USB3 10. UAE1/UAE2 NET SWAP 11. 內層+12V要打VIA在COMA處 12. SPDIFO_HDMI走12mil	
1.0	1. SATA2-SATA3文字面要隱藏 2. DART2 移至 DC_DQ1左上方 3. Q7 & DAR31 NET Change	
1.01	1. 0 OHM SHORT PAD (LAN & AUDIO) 2. DDR3 2400MHz OC modify (DDR3 DQ 走T型)	
1.02	1. DDR3 2400MHz OC modify (縮小DDR3間距)	
1.1	1. F.B "FB0603-RH" change to "FB0402-RH" 2. ATX_12V_2X2 change to ATX_12V_2X4 3. ARS105 LAN ARS101 CO-LAYOUT 4. Add pwok R200,BC9 放在ATX 端 5. msATA LAYOUT 龍華& FOXCONN CO-LAY(變更FOOTPRINT) 6. For USB3.0 eTron EJ168A 0.11um modify (UBU1 pin88/89) 7. add VCC1_05_PCH over voltage control	

BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990



LGA1155A

M_AAA0	AV27	SA_MA[0]	SA_DSQ[0]	AK3	M_DQSA0
M_AAA1	AY24	SA_MA[1]	SA_DSQ[0]	AK2	M_DQSA0
M_AAA2	AW24	SA_MA[2]			
M_AAA3	AW23	SA_MA[3]			
M_AAA4	AV23	SA_MA[4]	SA_DSQ[0]	AJ3	M_DA0
M_AAA5	AT24	SA_MA[5]	SA_DSQ[1]	AJ4	M_DA1
M_AAA6	AT23	SA_MA[6]	SA_DSQ[2]	AL3	M_DA2
M_AAA7	AU22	SA_MA[7]	SA_DSQ[3]	AL4	M_DA3
M_AAA8	AV22	SA_MA[8]	SA_DSQ[4]	AL2	M_DA4
M_AAA9	AT22	SA_MA[9]	SA_DSQ[5]	AJ1	M_DA5
M_AAA10	AV28	SA_MA[10]	SA_DSQ[6]	AL2	M_DA6
M_AAA11	AU21	SA_MA[11]	SA_DSQ[7]	AL1	M_DA7
M_AAA12	AT21	SA_MA[12]			
M_AAA13	AW32	SA_MA[13]	SA_DSQ[11]	AP3	M_DQSA1
M_AAA14	AU20	SA_MA[14]	SA_DSQ[11]	AP2	M_DQSA1
M_AAA15	AT20	SA_MA[15]			
[7] M_SWEA	M_SCASA	AV29	SA_WE#	AN1	M_DA8
[7] M_SCASA	M_SRASA	AV30	SA_DSQ[8]	AN4	M_DA9
[7] M_SRASA		AU28	SA_DSQ[9]	AR3	M_DA10
			SA_DSQ[10]	AR4	M_DA11
[7] M_SBA0	M_SBA0	AV29	SA_DSQ[11]	AR4	M_DA12
[7] M_SBA1	M_SBA1	AW28	SA_DSQ[12]	AN2	M_DA13
[7] M_SBA2	M_SBA2	AV20	SA_DSQ[13]	AN3	M_DA14
			SA_DSQ[14]	AR2	M_DA15
			SA_DSQ[15]	AR1	M_DA15
[7] M-CSA0	M-CSA0	AV29	SA_DSQ[2]	AW4	M_DQSA2
[7] M-CSA1	M-CSA1	AV32	SA_DSQ[2]	AW4	M_DQSA2
[7] M-CSA2	M-CSA2	AW30	SA_DSQ[2]	AW4	M_DQSA2
[7] M-CSA3	M-CSA3	AU33	SA_DSQ[2]	AW4	M_DQSA2
			SA_DSQ[3]		
[7] M_CKEA0	M_CKEA0	AV19	SA_DSQ[16]	AV2	M_DA16
[7] M_CKEA1	M_CKEA1	AT19	SA_DSQ[17]	AW3	M_DA17
[7] M_CKEA2	M_CKEA2	AU18	SA_DSQ[18]	AV5	M_DA18
[7] M_CKEA3	M_CKEA3	AV18	SA_DSQ[19]	AW5	M_DA19
			SA_DSQ[20]	AU2	M_DA20
			SA_DSQ[21]	AU3	M_DA21
			SA_DSQ[22]	AU5	M_DA22
			SA_DSQ[23]	AY5	M_DA23
			SA_DSQ[3]	AV8	M_DQSA3
			SA_DSQ[3]	AW8	M_DQSA3
[7] M_DCLKA0	M_DCLKA0	AY25	SA_DSQ[24]	AY7	M_DA24
[7] M_DCLKA0	M_DCLKA0	AW25	SA_DSQ[25]	AU7	M_DA25
[7] M_DCLKA1	M_DCLKA1	AU24	SA_DSQ[26]	AU9	M_DA26
[7] M_DCLKA1	M_DCLKA1	AU25	SA_DSQ[27]	AY7	M_DA27
[7] M_DCLKA2	M_DCLKA2	AW27	SA_DSQ[28]	AW7	M_DA28
[7] M_DCLKA2	M_DCLKA2	AY27	SA_DSQ[29]	AW9	M_DA29
[7] M_DCLKA3	M_DCLKA3	AW28	SA_DSQ[30]	AY9	M_DA30
[7] M_DCLKA3	M_DCLKA3	AW28	SA_DSQ[31]	AY9	M_DA31
			SA_DSQ[4]	AV37	M_DQSA4
			SA_DSQ[4]	AV36	M_DQSA4
			SA_DSQ[32]	AU35	M_DA32
			SA_DSQ[33]	AW37	M_DA33
			SA_DSQ[34]	AU39	M_DA34
			SA_DSQ[35]	AU36	M_DA35
			SA_DSQ[36]	AW35	M_DA36
			SA_DSQ[37]	AY36	M_DA37
			SA_DSQ[38]	AU38	M_DA38
			SA_DSQ[39]	AU37	M_DA39
			SA_DSQ[5]	AP38	M_DQSA5
			SA_DSQ[5]	AP39	M_DQSA5
			SA_DSQ[40]	AR40	M_DA40
			SA_DSQ[41]	AR37	M_DA41
			SA_DSQ[42]	AN38	M_DA42
			SA_DSQ[43]	AN37	M_DA43
			SA_DSQ[44]	AR39	M_DA44
			SA_DSQ[45]	AR38	M_DA45
			SA_DSQ[46]	AN39	M_DA46
			SA_DSQ[47]	AN40	M_DA47
			SA_DSQ[6]	AK38	M_DQSA6
			SA_DSQ[6]	AK39	M_DQSA6
			SA_DSQ[48]	AL40	M_DA48
			SA_DSQ[49]	AL37	M_DA49
			SA_DSQ[50]	AJ38	M_DA50
			SA_DSQ[51]	AJ37	M_DA51
			SA_DSQ[52]	AL39	M_DA52
			SA_DSQ[53]	AL38	M_DA53
			SA_DSQ[54]	AJ39	M_DA54
			SA_DSQ[55]	AJ40	M_DA55
			SA_DSQ[7]	AF38	M_DQSA7
			SA_DSQ[7]	AF39	M_DQSA7
			SA_DSQ[56]	AG40	M_DA56
			SA_DSQ[57]	AG37	M_DA57
			SA_DSQ[58]	AE38	M_DA58
			SA_DSQ[59]	AE37	M_DA59
			SA_DSQ[60]	AG39	M_DA60
			SA_DSQ[61]	AG38	M_DA61
			SA_DSQ[62]	AE39	M_DA62
			SA_DSQ[63]	AE40	M_DA63

DDR_0

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LGA1155[10SC1-F01155-01R]

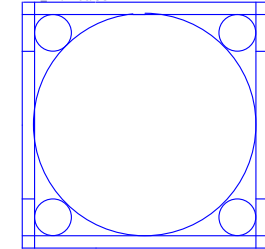
LGA1155B

M_AAB0	AK24	SB_MA[0]	SB_DSQ[0]	AH7	M_DQSB0
M_AAB1	AM20	SB_MA[1]	SB_DSQ[0]	AH6	M_DQSB0
M_AAB2	AM19	SB_MA[2]			
M_AAB3	AK18	SB_MA[3]			
M_AAB4	AP19	SB_MA[4]	SB_DSQ[0]	AG7	M_D80
M_AAB5	AP18	SB_MA[5]	SB_DSQ[1]	AG8	M_D81
M_AAB6	AM18	SB_MA[6]	SB_DSQ[2]	AJ9	M_D82
M_AAB7	AL18	SB_MA[7]	SB_DSQ[3]	AJ8	M_D83
M_AAB8	AY17	SB_MA[8]	SB_DSQ[4]	AG5	M_D84
M_AAB9	AN18	SB_MA[9]	SB_DSQ[5]	AG6	M_D85
M_AAB10	AN13	SB_MA[10]	SB_DSQ[6]	AJ6	M_D86
M_AAB11	AU17	SB_MA[11]	SB_DSQ[7]	AJ7	M_D87
M_AAB12	AT18	SB_MA[12]			
M_AAB13	AR26	SB_MA[13]	SB_DSQ[11]	AM8	M_DQSB1
M_AAB14	AY16	SB_MA[14]	SB_DSQ[11]	AL8	M_DQSB1
M_AAB15	AV16	SB_MA[15]			
[8] M_SWEB	M_SWEB	AR25	SB_DSQ[8]	AL7	M_D88
[8] M_SCASB	M_SCASB	AK25	SB_DSQ[9]	AM7	M_D89
[8] M_SRASB	M_SRASB	AP24	SB_DSQ[10]	AM10	M_D90
			SB_DSQ[11]	AL10	M_D91
			SB_DSQ[12]	AL6	M_D92
			SB_DSQ[13]	AM6	M_D93
			SB_DSQ[14]	AL9	M_D94
			SB_DSQ[15]	AM9	M_D95
[8] M-CSB0	M-CSB0	AN25	SB_DSQ[2]	AR8	M_DQSB2
[8] M-CSB1	M-CSB1	AN26	SB_DSQ[2]	AP8	M_DQSB2
[8] M-CSB2	M-CSB2	AL25	SB_DSQ[2]		
[8] M-CSB3	M-CSB3	AT26	SB_DSQ[3]		
			SB_DSQ[16]	AP7	M_D96
			SB_DSQ[17]	AR7	M_D97
			SB_DSQ[18]	AR10	M_D98
			SB_DSQ[19]	AR10	M_D99
			SB_DSQ[20]	AP6	M_D100
			SB_DSQ[21]	AR6	M_D101
			SB_DSQ[22]	AP9	M_D102
			SB_DSQ[23]	AR9	M_D103
			SB_DSQ[3]	AN13	M_DQSB3
			SB_DSQ[3]	AN12	M_DQSB3
[8] M_DCLKB0	M_DCLKB0	AL21	SB_DSQ[24]	AM12	M_D104
[8] M_DCLKB0	M_DCLKB0	AL22	SB_DSQ[25]	AM13	M_D105
[8] M_DCLKB1	M_DCLKB1	AK20	SB_DSQ[26]	AR13	M_D106
[8] M_DCLKB2	M_DCLKB2	AL23	SB_DSQ[27]	AP13	M_D107
[8] M_DCLKB2	M_DCLKB2	AM22	SB_DSQ[28]	AL12	M_D108
[8] M_DCLKB3	M_DCLKB3	AP21	SB_DSQ[29]	AL13	M_D109
[8] M_DCLKB3	M_DCLKB3	AN21	SB_DSQ[30]	AR12	M_D110
			SB_DSQ[31]	AP12	M_D111
			SB_DSQ[4]	AN29	M_DQSB4
			SB_DSQ[4]	AN28	M_DQSB4
			SB_DSQ[32]	AR28	M_D112
			SB_DSQ[33]	AR29	M_D113
			SB_DSQ[34]	AL28	M_D114
			SB_DSQ[35]	AL29	M_D115
			SB_DSQ[36]	AP28	M_D116
			SB_DSQ[37]	AP29	M_D117
			SB_DSQ[38]	AM28	M_D118
			SB_DSQ[39]	AM29	M_D119
			SB_DSQ[5]	AP33	M_DQSB5
			SB_DSQ[5]	AR33	M_DQSB5
			SB_DSQ[40]	AP32	M_D120
			SB_DSQ[41]	AP31	M_D121
			SB_DSQ[42]	AP34	M_D122
			SB_DSQ[43]	AR32	M_D123
			SB_DSQ[44]	AR31	M_D124
			SB_DSQ[45]	AR35	M_D125
			SB_DSQ[46]	AR34	M_D126
			SB_DSQ[47]	AL33	M_DQSB6
			SB_DSQ[47]	AM33	M_DQSB6
			SB_DSQ[48]	AM32	M_D127
			SB_DSQ[49]	AL35	M_D128
			SB_DSQ[50]	AL32	M_D129
			SB_DSQ[51]	AM34	M_D130
			SB_DSQ[52]	AL31	M_D131
			SB_DSQ[53]	AM35	M_D132
			SB_DSQ[54]	AL34	M_D133
			SB_DSQ[55]		
			SB_DSQ[7]	AG35	M_DQSB7
			SB_DSQ[7]	AG34	M_DQSB7
			SB_DSQ[56]	AH35	M_D134
			SB_DSQ[57]	AH34	M_D135
			SB_DSQ[58]	AE34	M_D136
			SB_DSQ[59]	AE35	M_D137
			SB_DSQ[60]	AJ35	M_D138
			SB_DSQ[61]	AJ34	M_D139
			SB_DSQ[62]	AE33	M_D140
			SB_DSQ[63]	AE33	M_D141

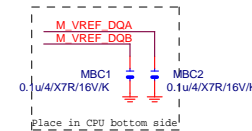
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LGA1155[10SC1-F01155-01R]

LGA1155
ILM BP/1156/CSP

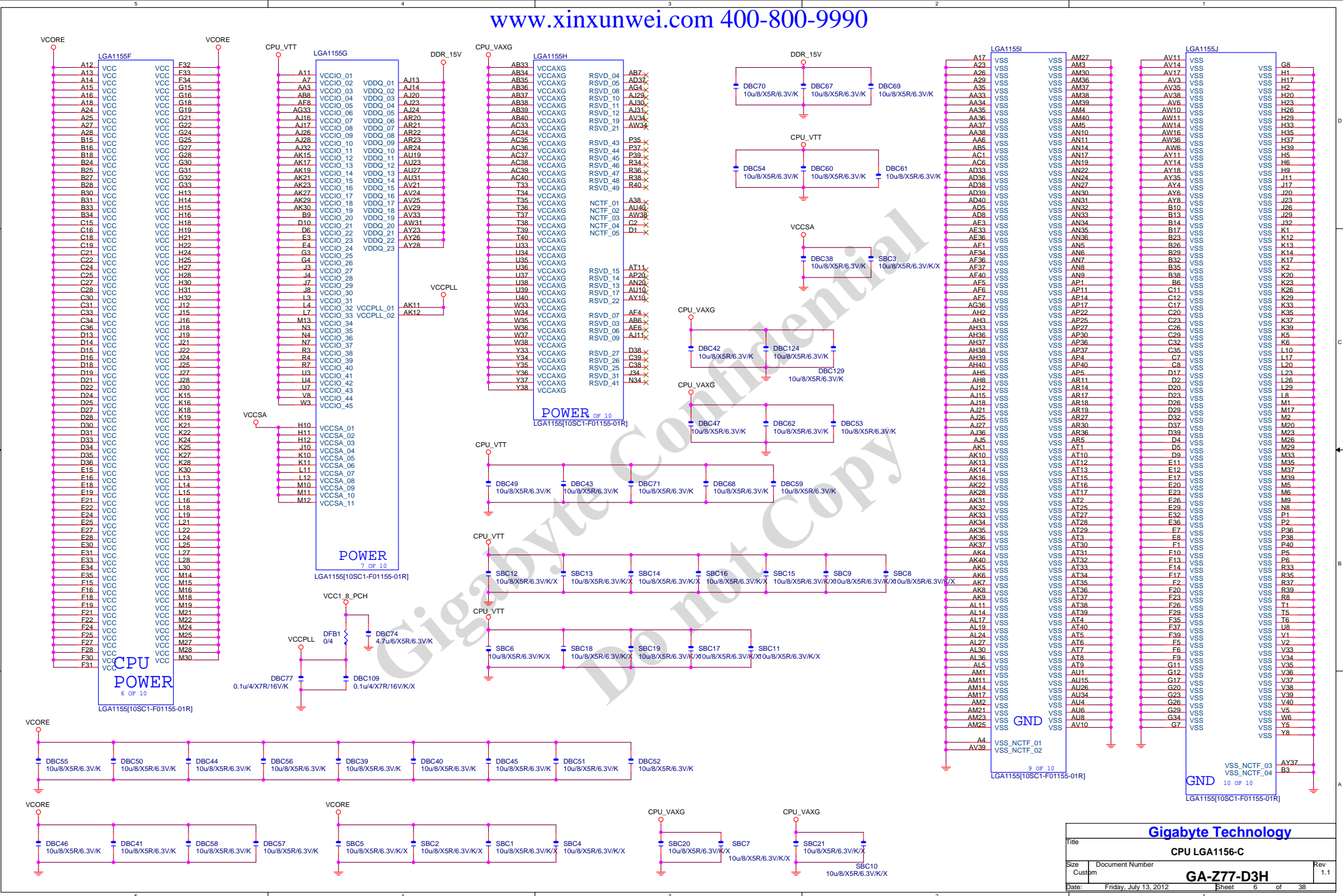
Need check the new CPU ME

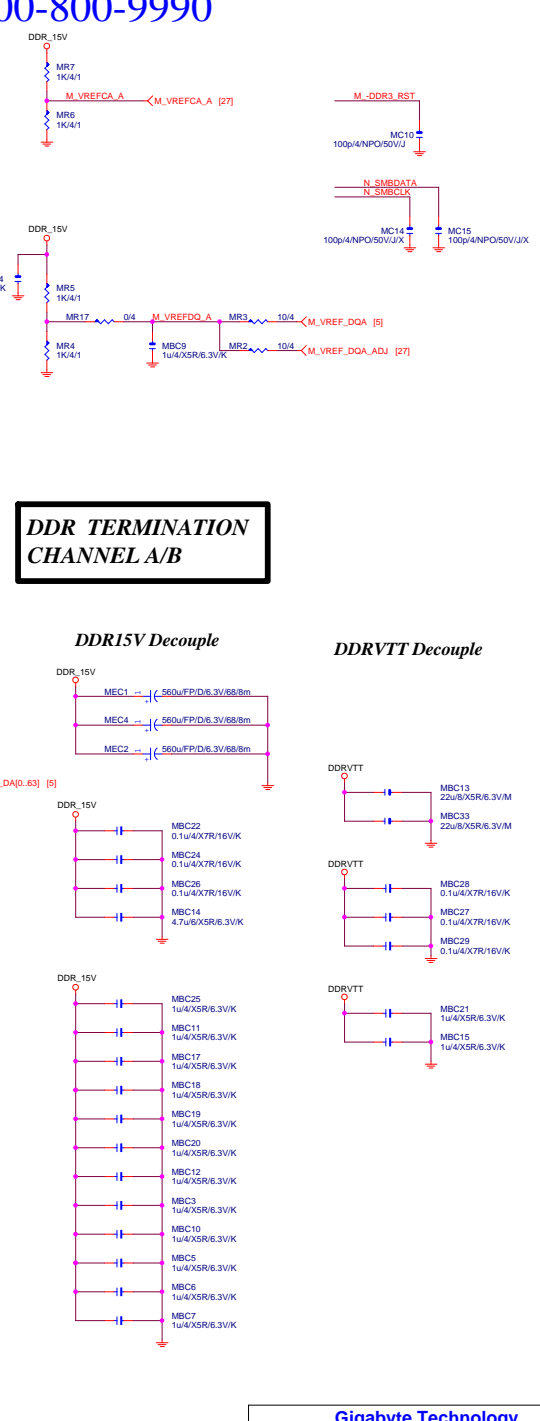
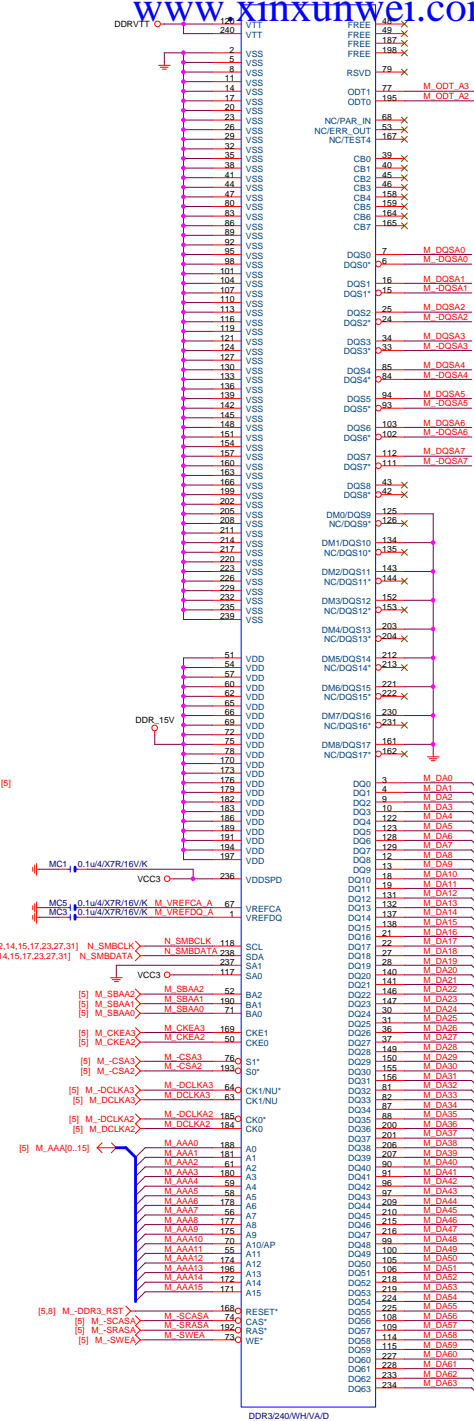
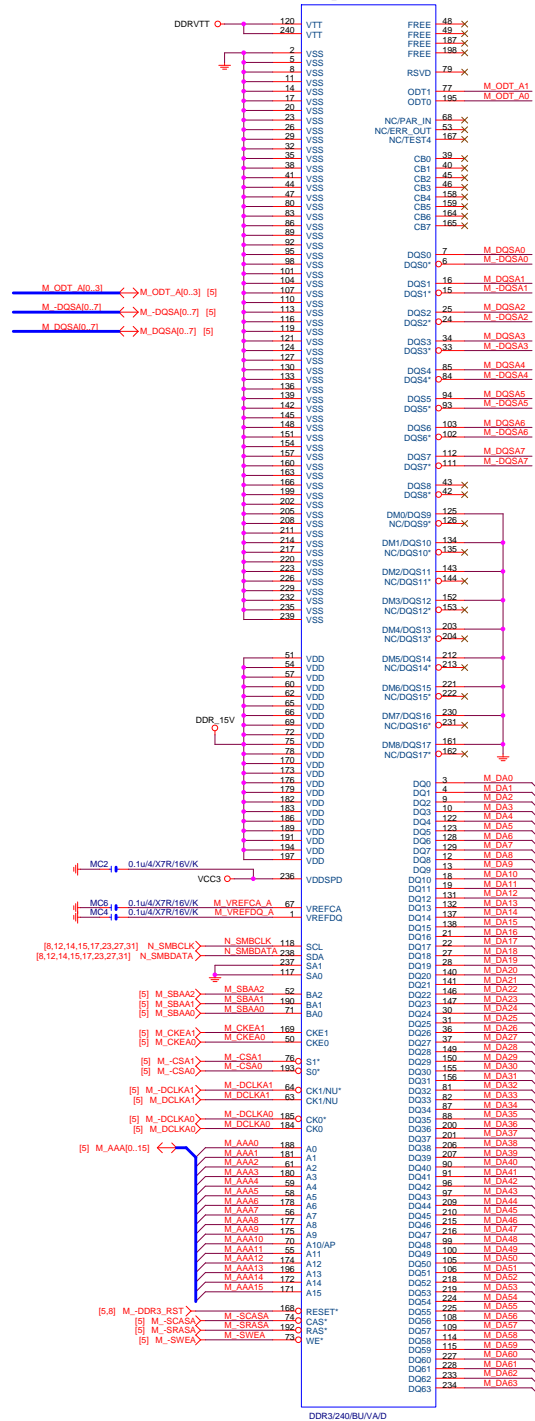


Gigabyte Technology

CPU LGA1156-B

Title			CPU LGA1156-B		
Size			Document Number		
Custom			GA-Z77-D3H		
Date:			Friday, July 13, 2012		
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			Rev 1.1		

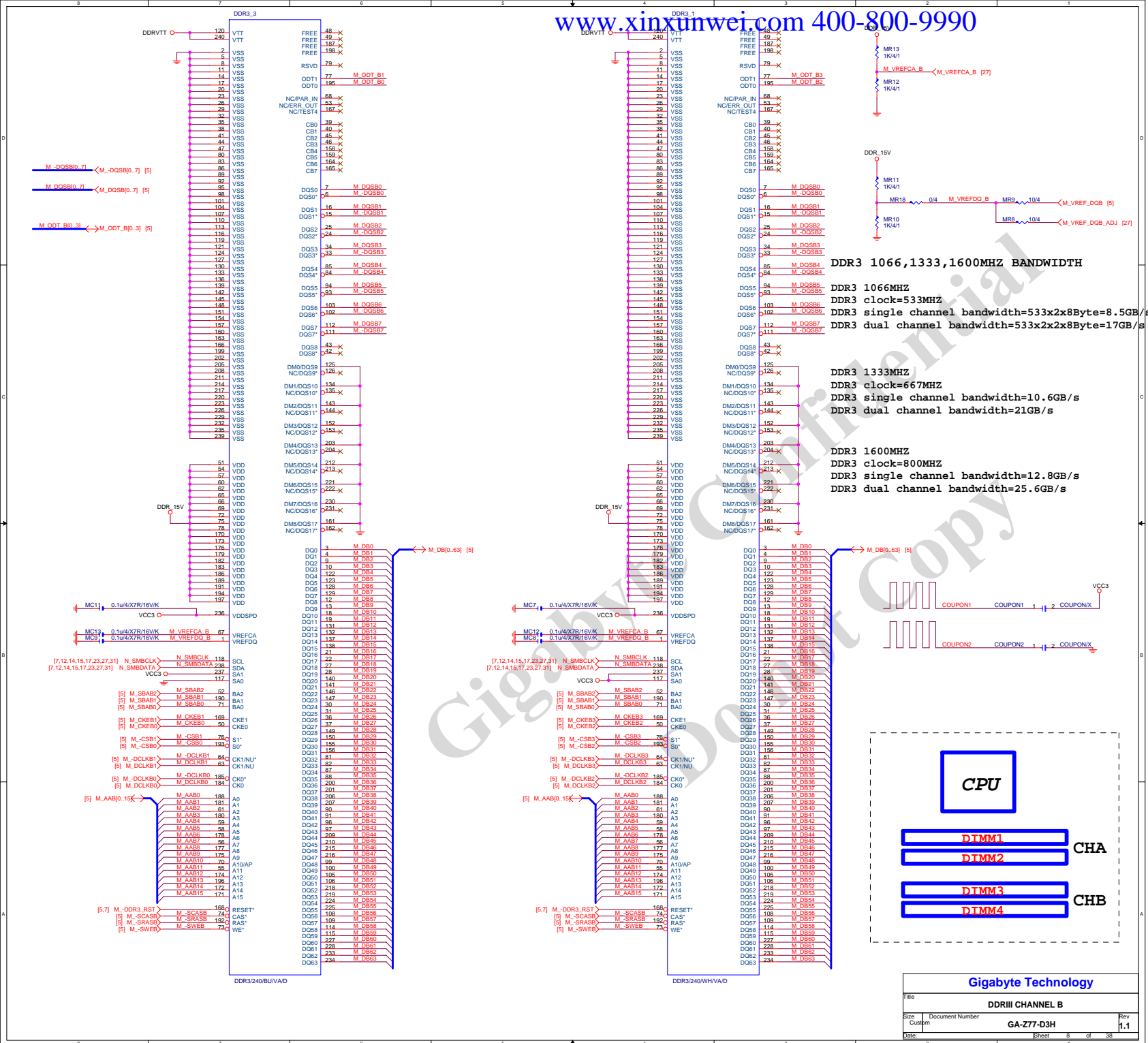




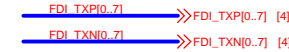
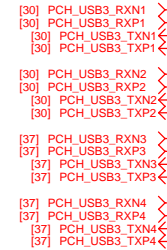
**DDR TERMINATION
CHANNEL A/B**

DDR15V Decouple

DDRVTT Decouple



Impedance=85 +/- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS



```

F [30] OC[3:0]# for
      Device 29
      (ports 0-7)
R [30,33] OC[7:4]# for
      Device 26
      (ports 8-13)

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[illegible]

VCC1_8_PCH

NR118
2.2K/4/1

NR117
4.7K/4 N_NV_CLE

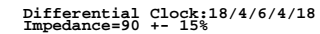
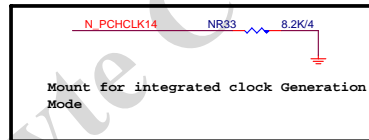
A_H_SNB [4]

DMI / FDI termination voltage

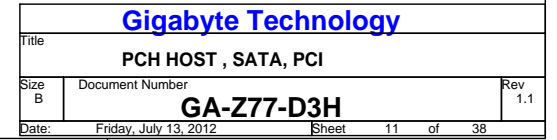
NBC57
0.1u/4/X7R/16V/K

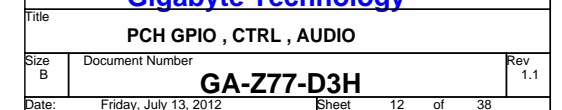
Mount for integrated clock Generation Mode

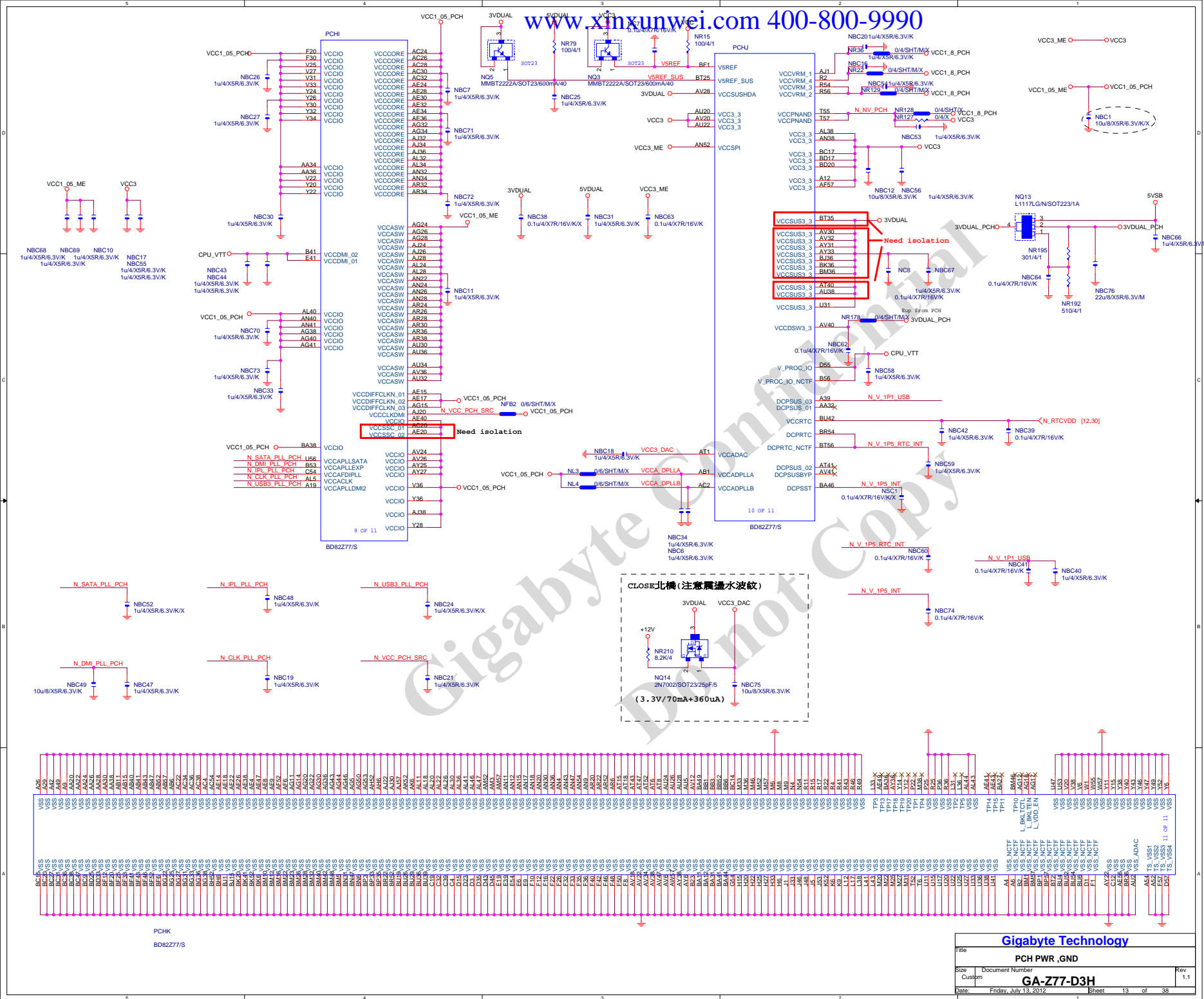
Title			
PCH FDI,DMI,USB ,PCIE			
Size	Document Number	Rev	
Custom	GA-Z77-D3H	1.1	
Date:	Friday, July 13, 2012	Sheet	9 of 38

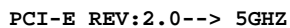


NR64 8.2K/4/X N_GPIO17
NR173 8.2K/4/X N_GPIO19

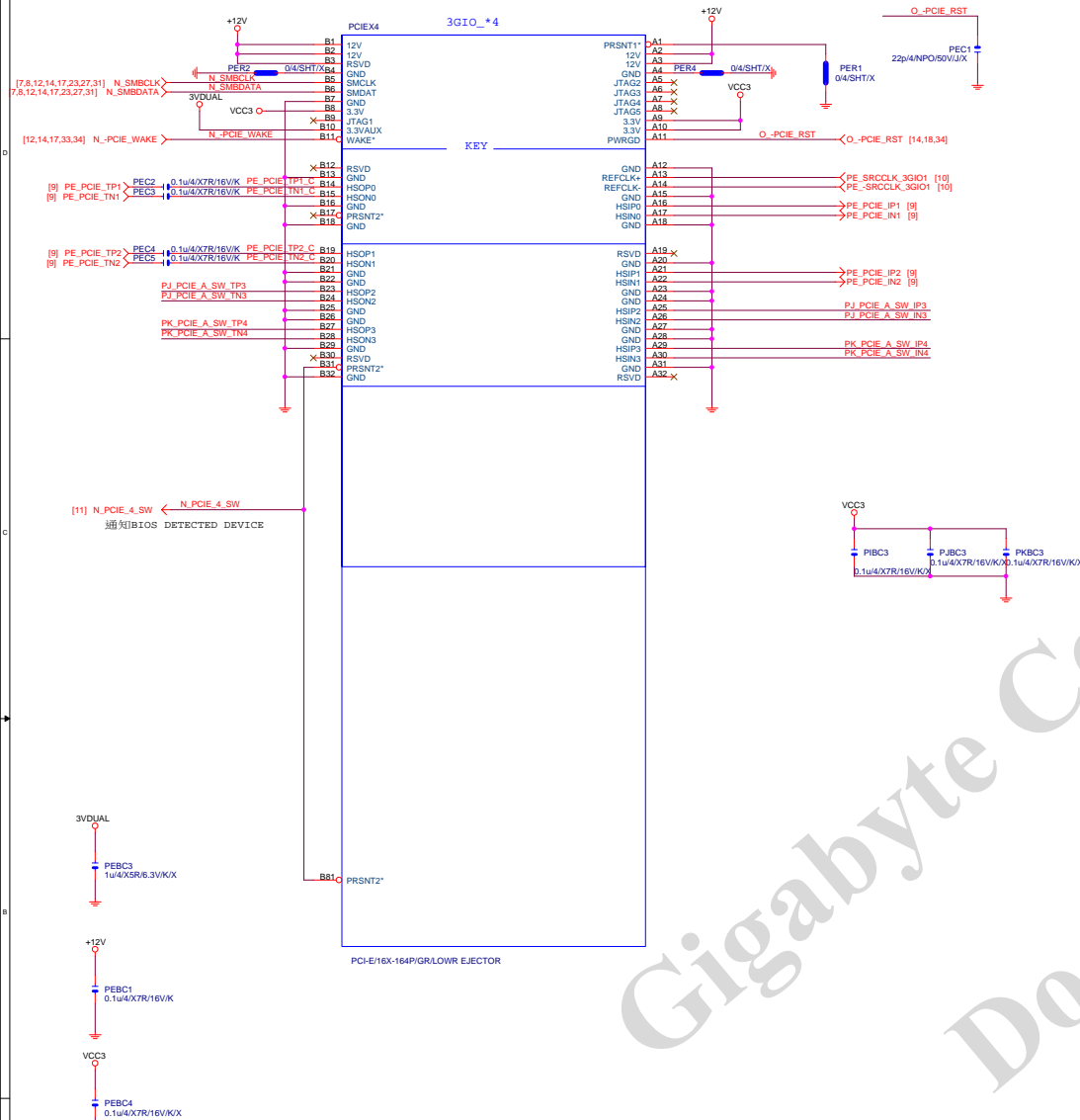








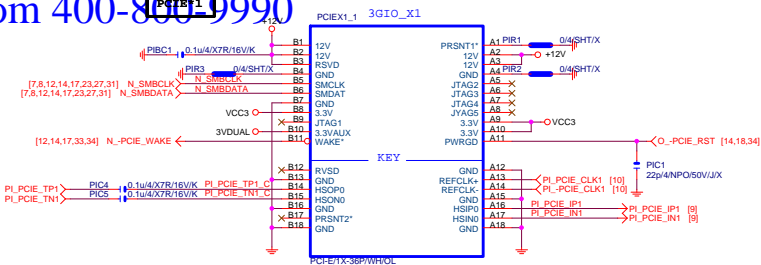
PCIE*4



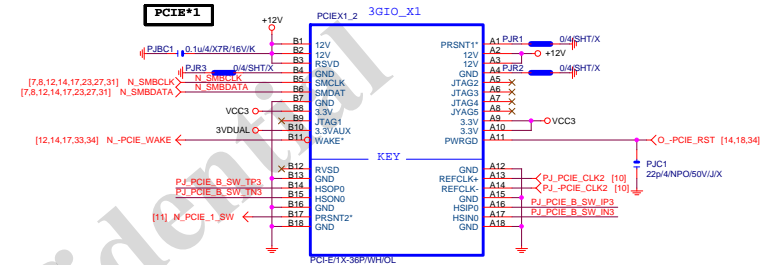
N_PCIE_4_SW (PCH GPIO38) PCIE4_X1 (SIO GPIO26)

PCIE1,PCIE4 --> X1 (Default)	H	H
PCIE4 No devices	H	H
PCIE4 --> X1		
PCIE4 Have devices		
PCIE4 --> X4	L	L
PCIE1_2/PCIE1_3 --> N/A		

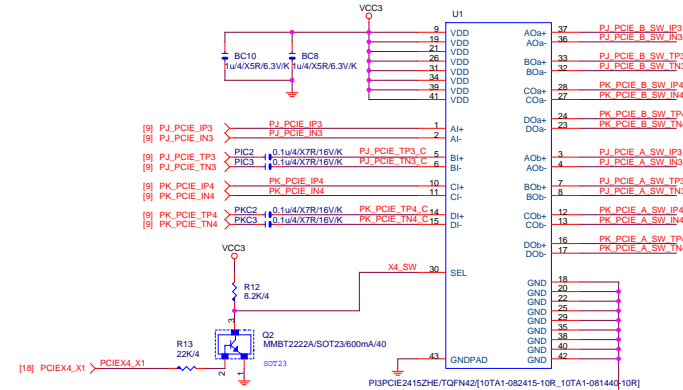
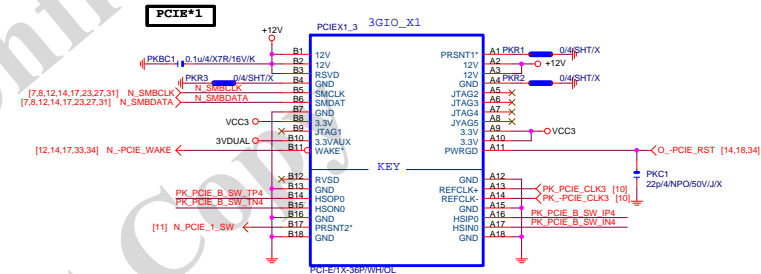
PCIE*1



PCIE*1



PCIE*1



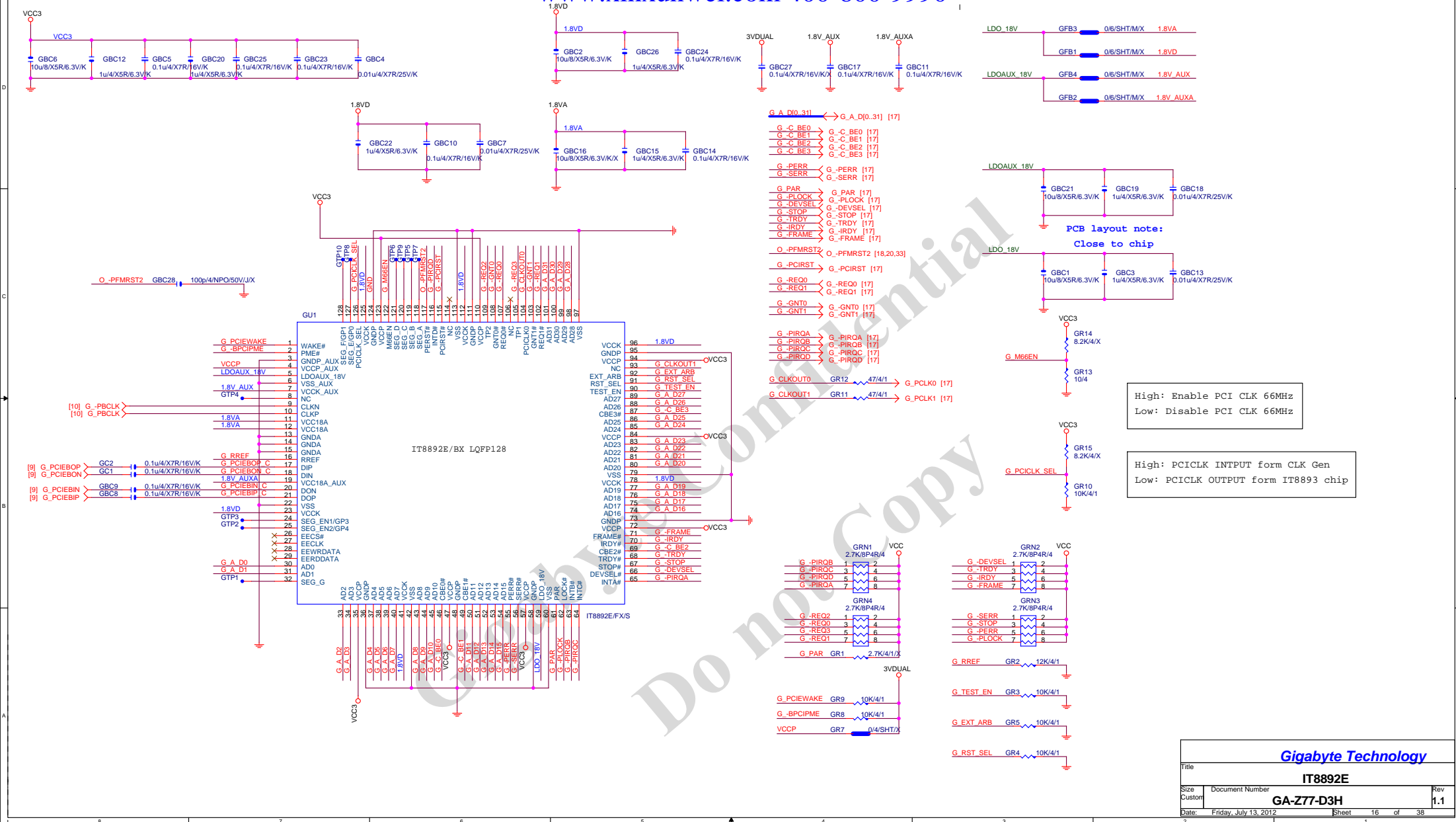
Function	SEL
X1--> x0a	L ₁ PCIE4 SLOT-->X1
X1--> x0b	H ₁ PCIE4 SLOT-->X4

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PCIE_X1_1.2

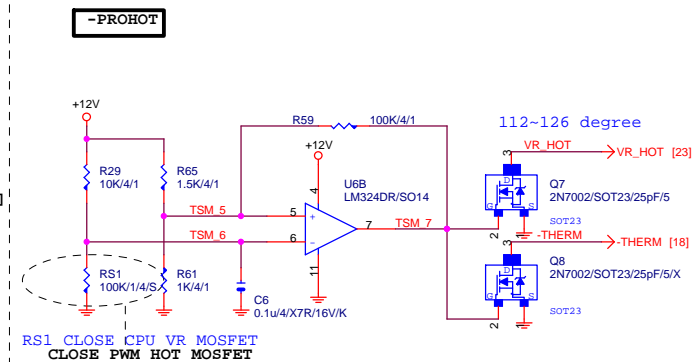
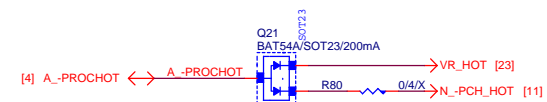
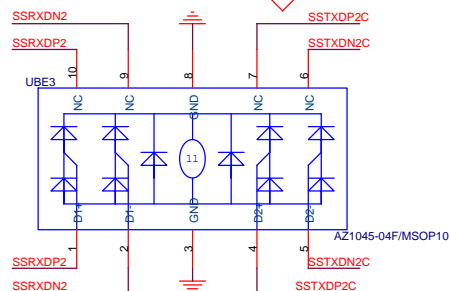
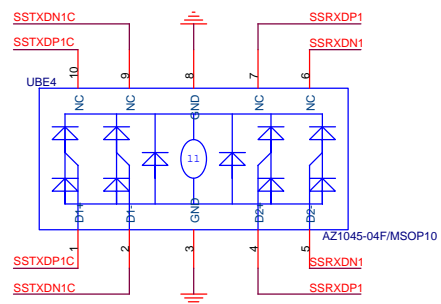
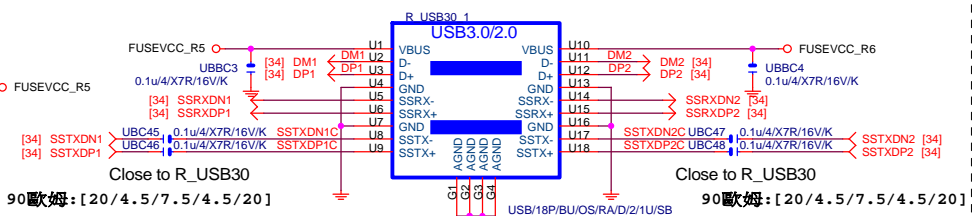
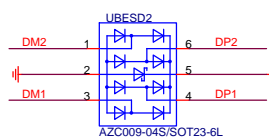
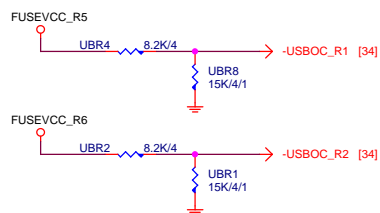
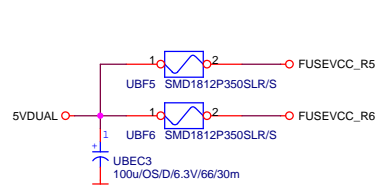
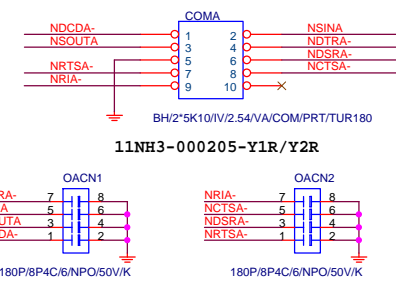
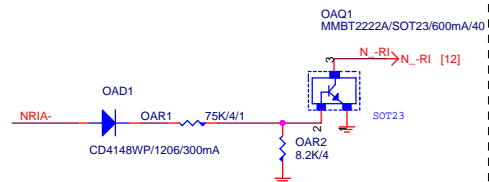
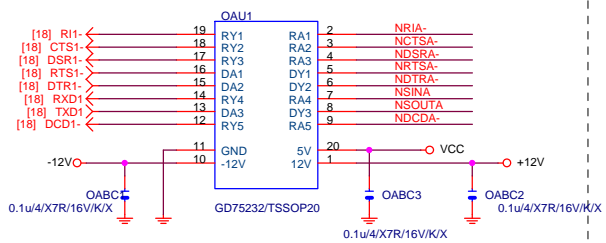
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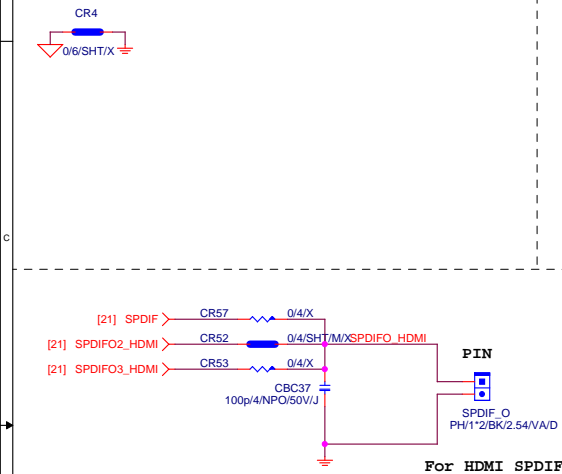
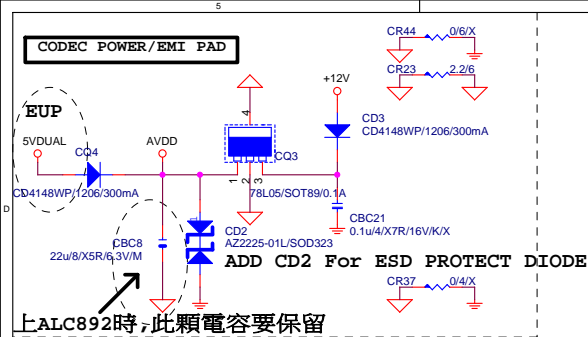
COM RI



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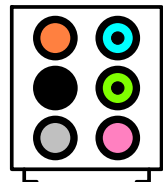

```
CR36: 20K/4/1% @Realtek cdec & VT1708S-CE
CR36: 5.1K/4/1 @VIA codec VT1708S-CD/VT2021
CBC38 100P @VIA codec VT1708S
```



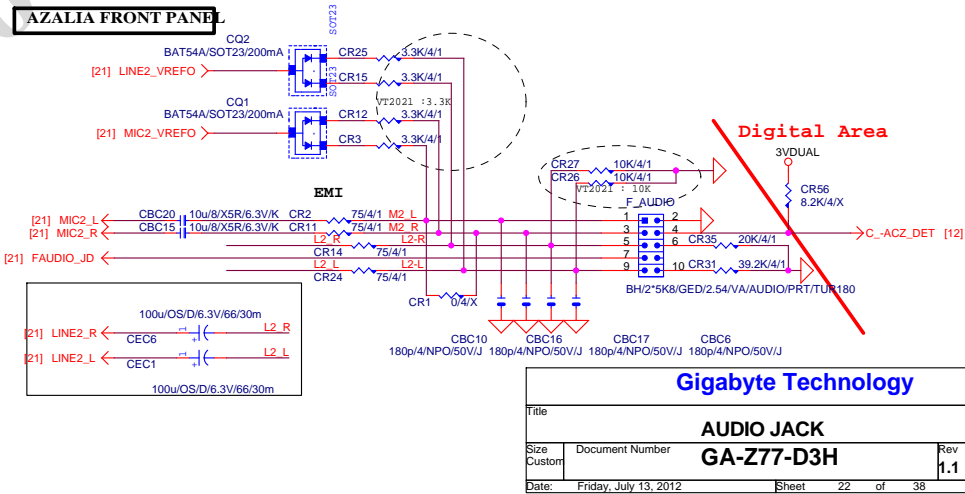
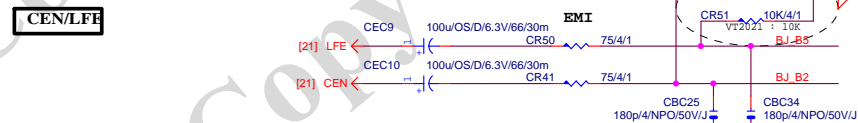
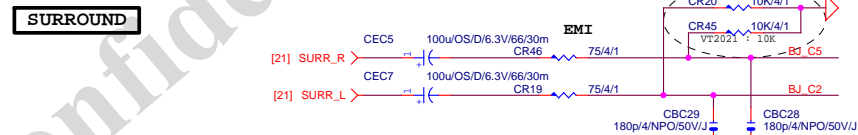
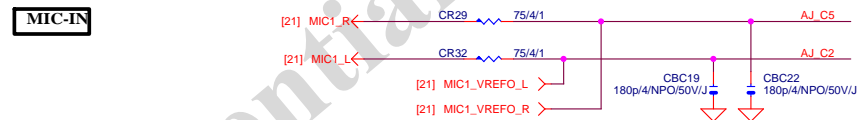
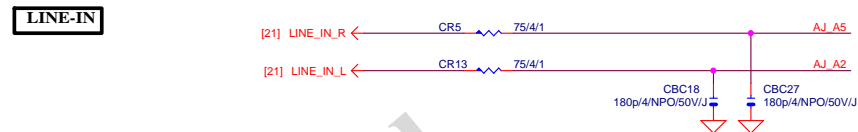
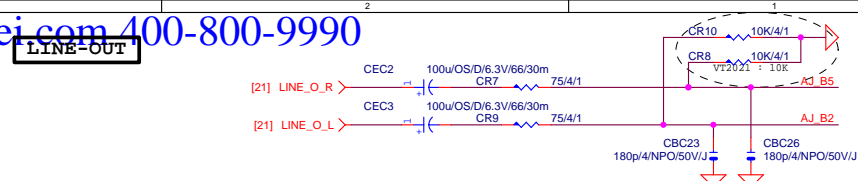
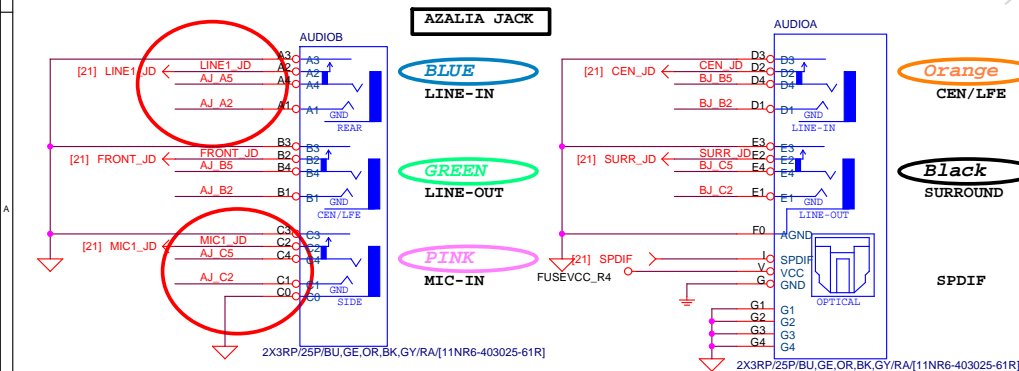


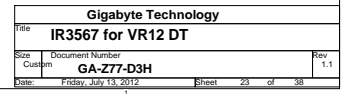
AZALIA JACK

BTX AZALIA CONNECTOR

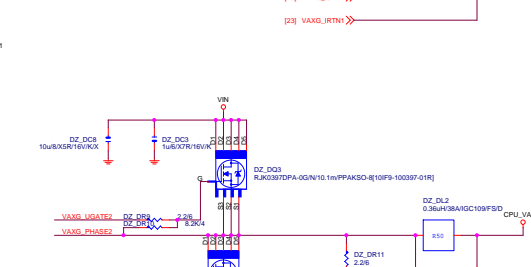


11NR6-403007-21R





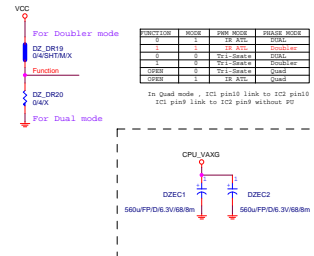
VAXG Phase



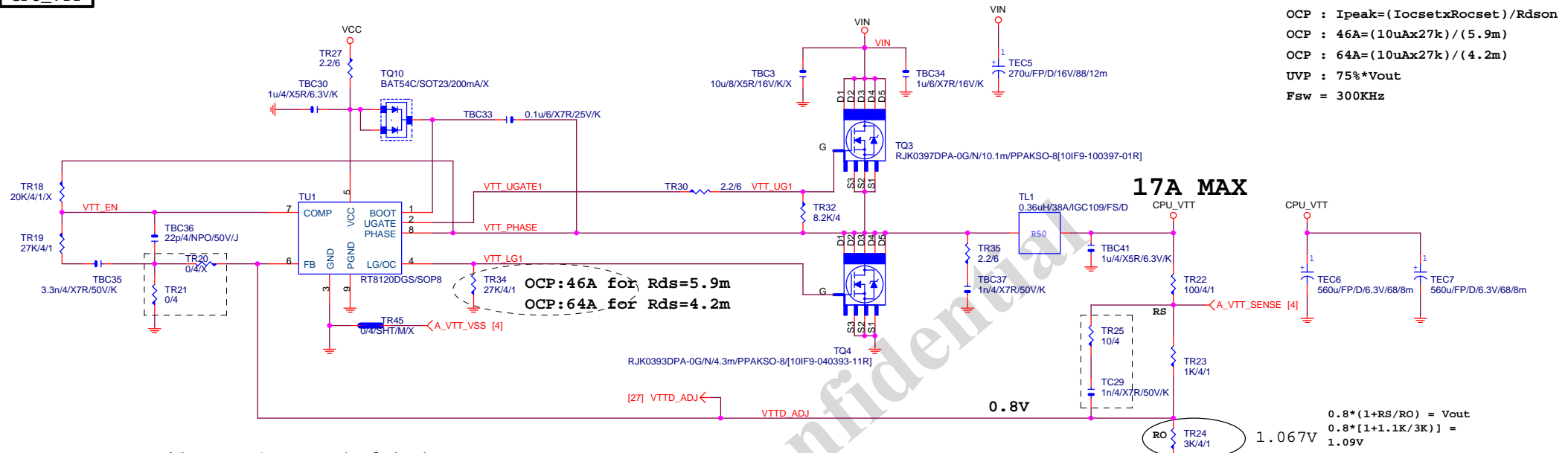
FUNCTION	MODE	PWM MODE	PHASE MOD
0	1	IR ATL	DUAL
1	1	IR ATL	Doubles
0	0	Tri-Scate	DUAL
1	0	Tri-Scate	Doubles
OPEN	0	Tri-Scate	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without 50

VAXG PHASE 1,2

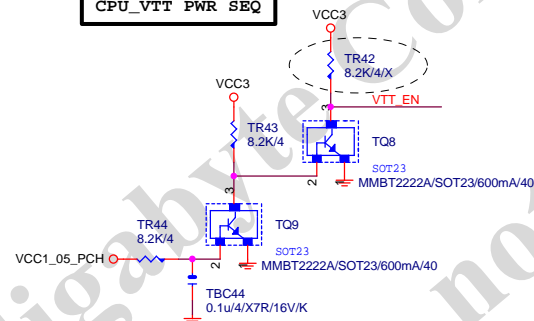


CPU_VTT



$$OCP: 46A = \frac{R_{oset} * I_{ocset}}{R_{ds(on)}} = \frac{27K * 10uA}{5.9m}$$

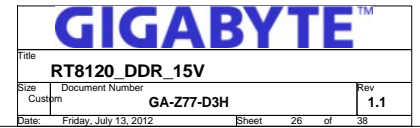
CPU_VTT PWR SEQ

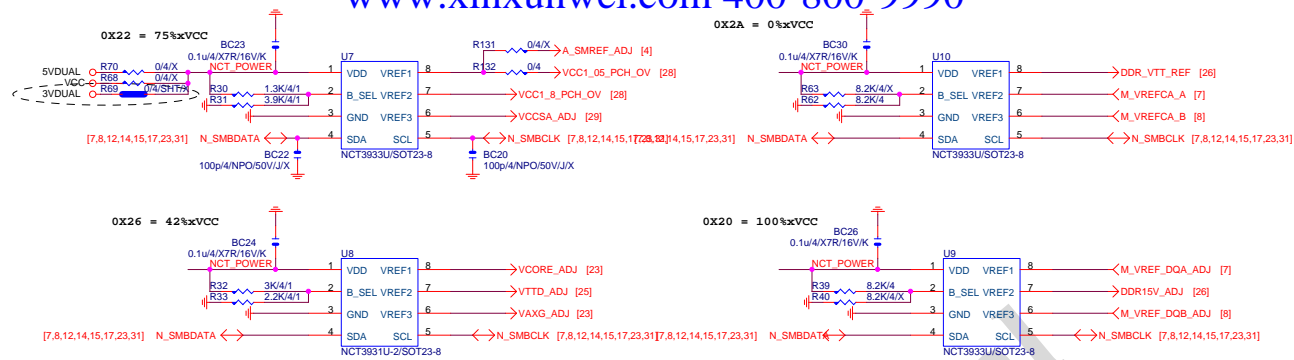


	VTT_SEL
HI	1.05V
LO	1.0V

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RT8120_CPU_VTT		
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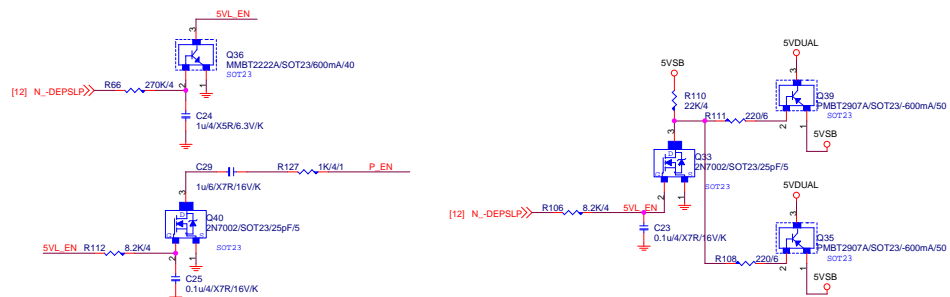
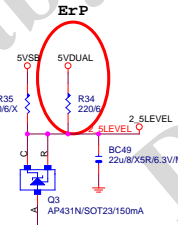
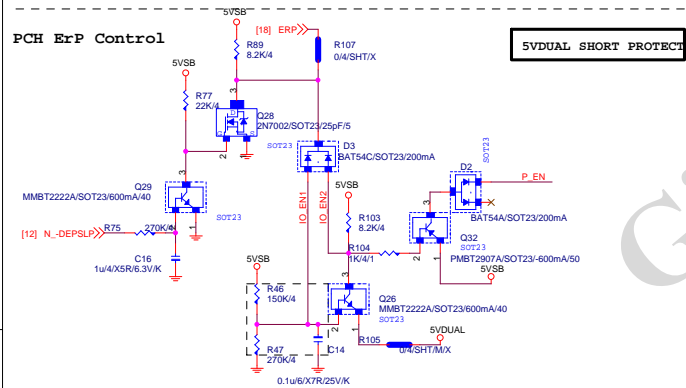
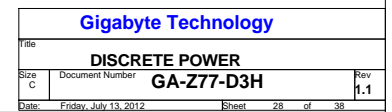
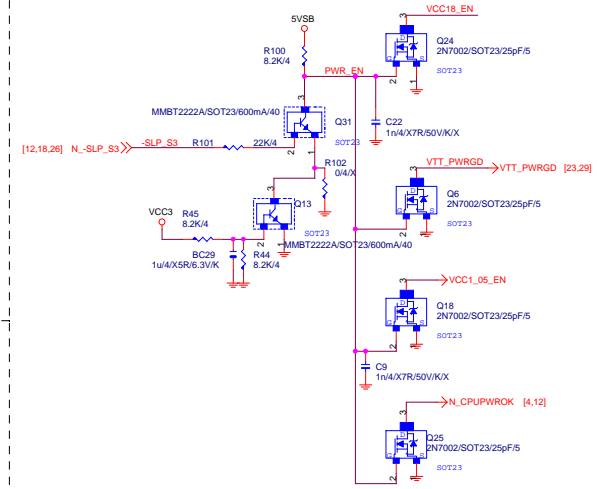
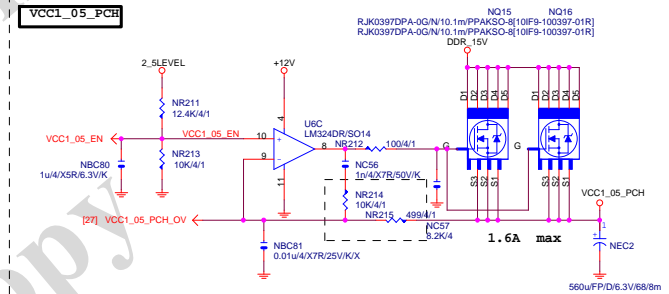
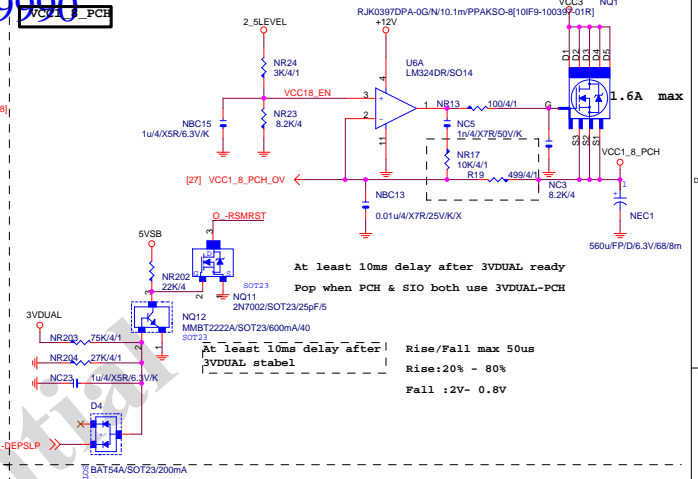
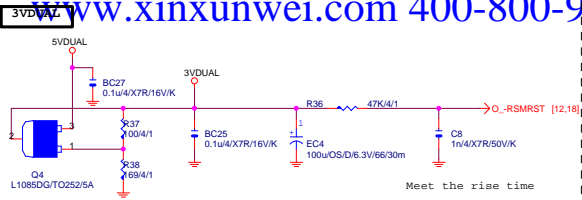
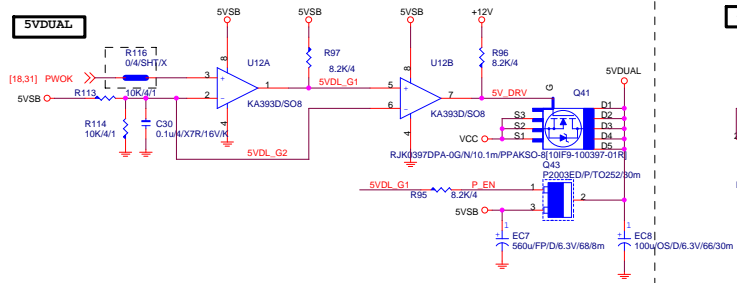




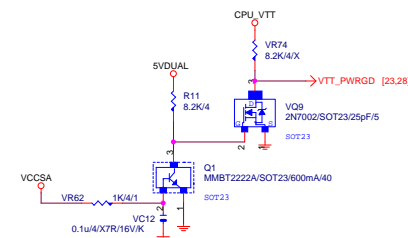
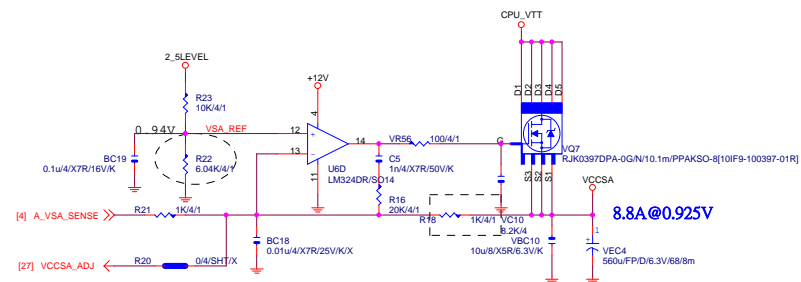
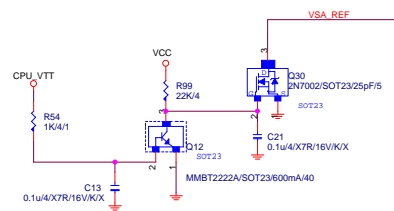
NCT3933	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	SMREF	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	CPU_VTT
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	VCCSA	VAXG

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VCC_SA



Gigabyte Technology

CPU VTT PWM_ISL6312

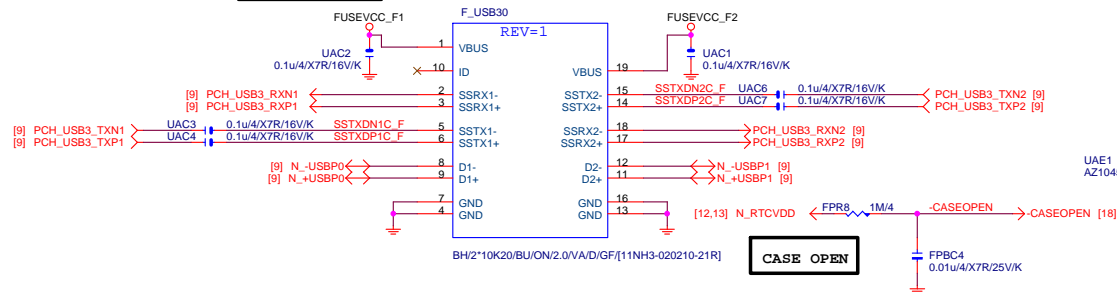
GA-Z77-D3H

Date: Friday, July 13, 2012

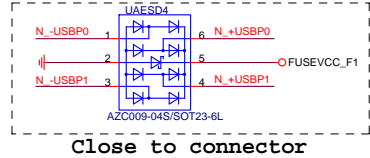
Sheet 29 of 38

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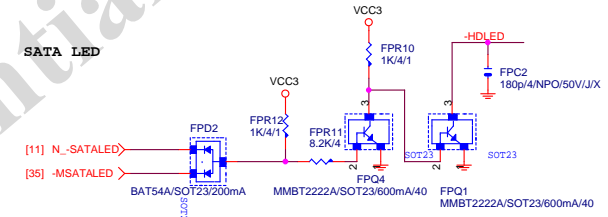
Front USB3.0



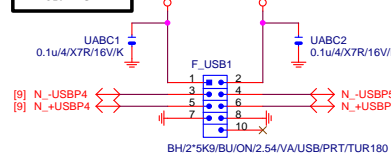
BLUE



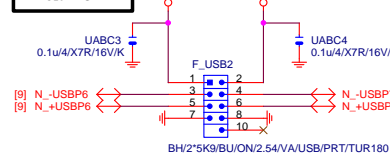
SATA LED



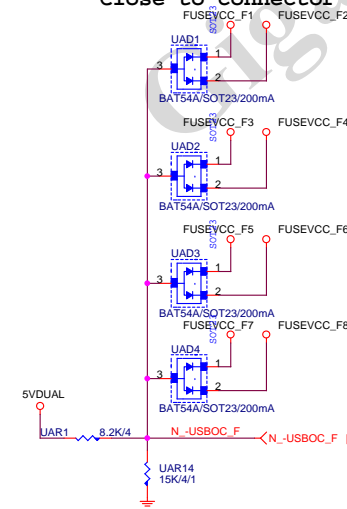
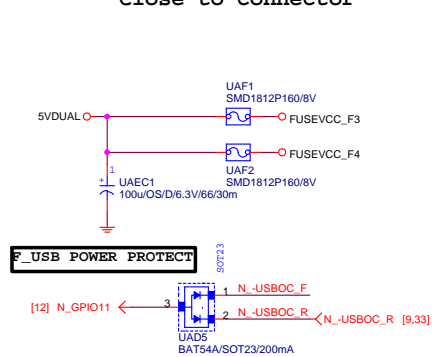
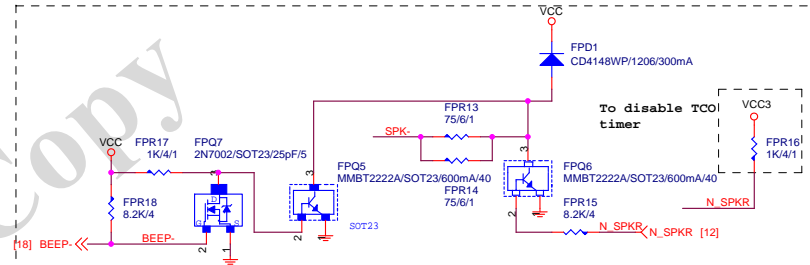
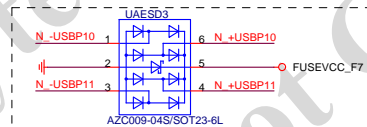
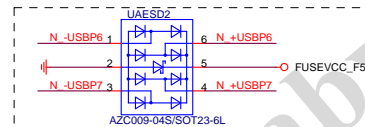
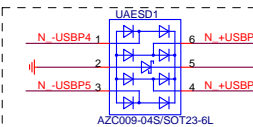
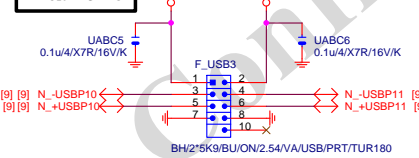
FRONT USB2



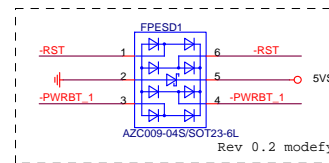
FRONT USB2



FRONT USB3

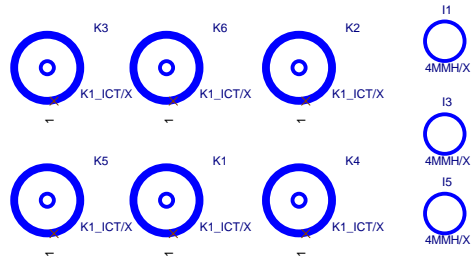
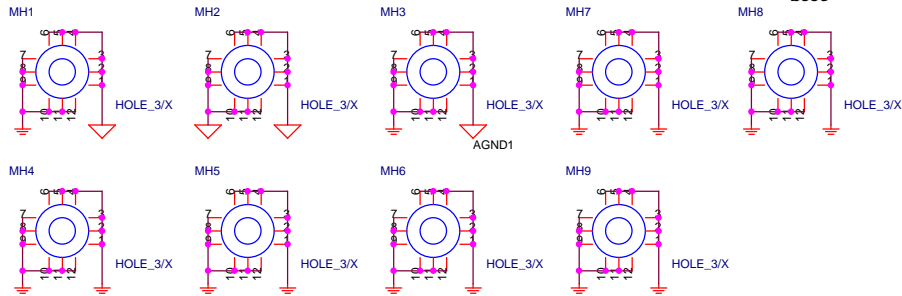
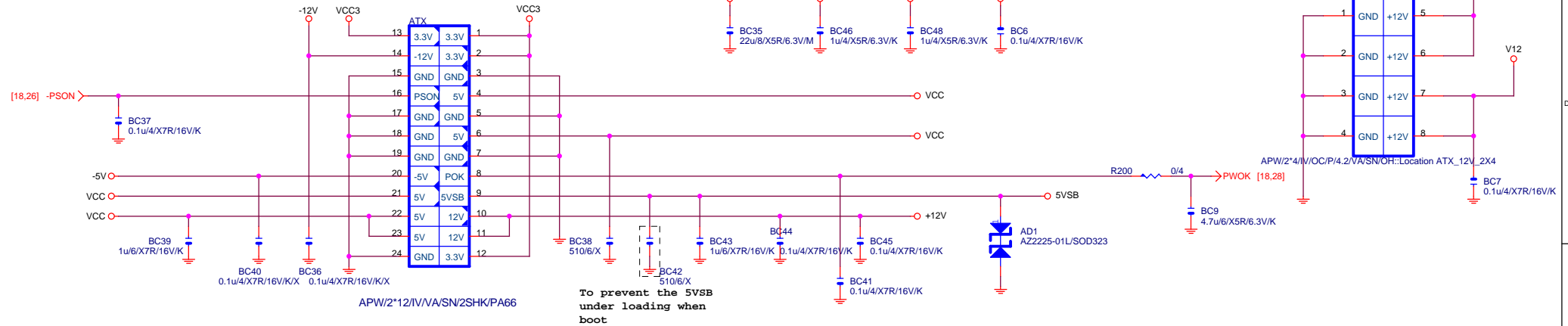


INTEL FRONT PANEL

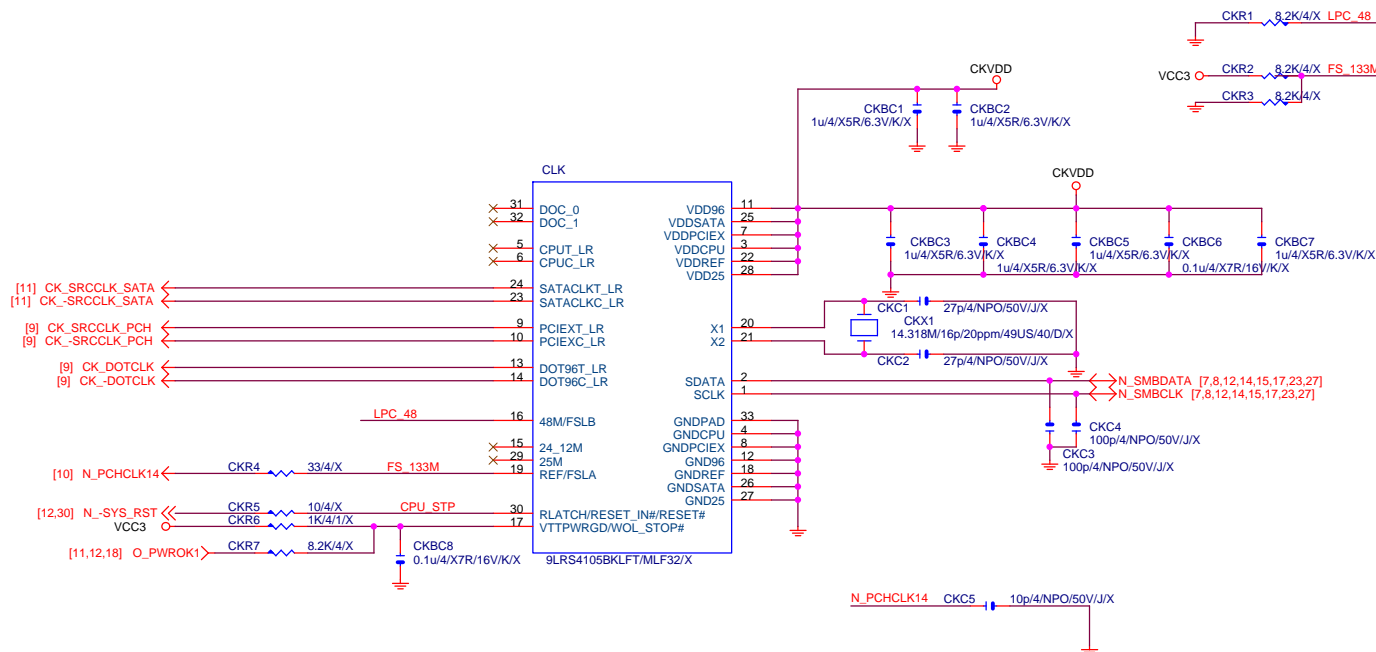


ATX POWER CONNECTOR

www.xinxunwei.com 400-800-9990

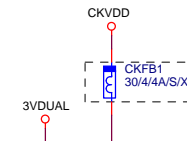


CLK GEN



CPU Frequency Selection

FS	CPU
0	100M <Default>
1	133M

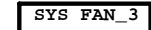


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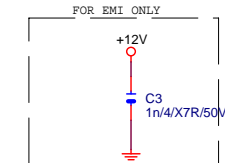
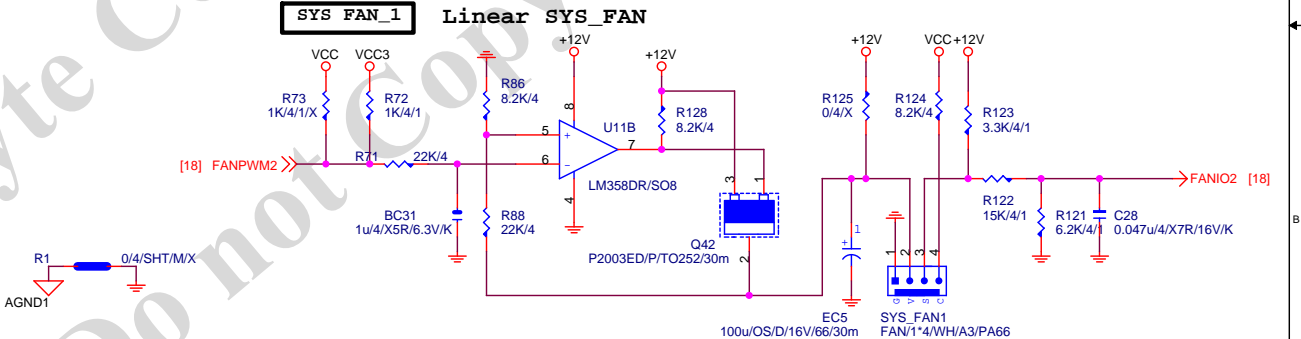
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```
* IT8728 BX      VIN2 must +12V input
** IT8728 CX     VIN3 must VCC input
```



SYS_FAN_1 Linear SYS_FAN



LAN POWER

AR8161: LAR5(O), LAR3/LAR4(X)

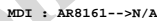
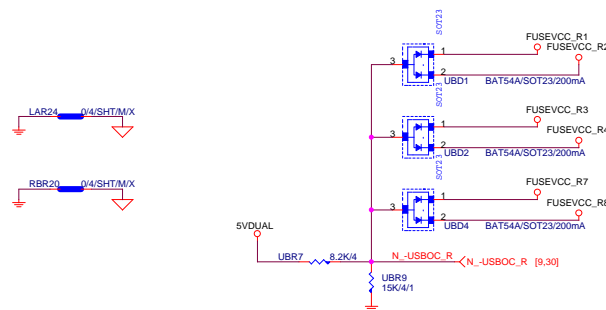
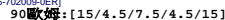
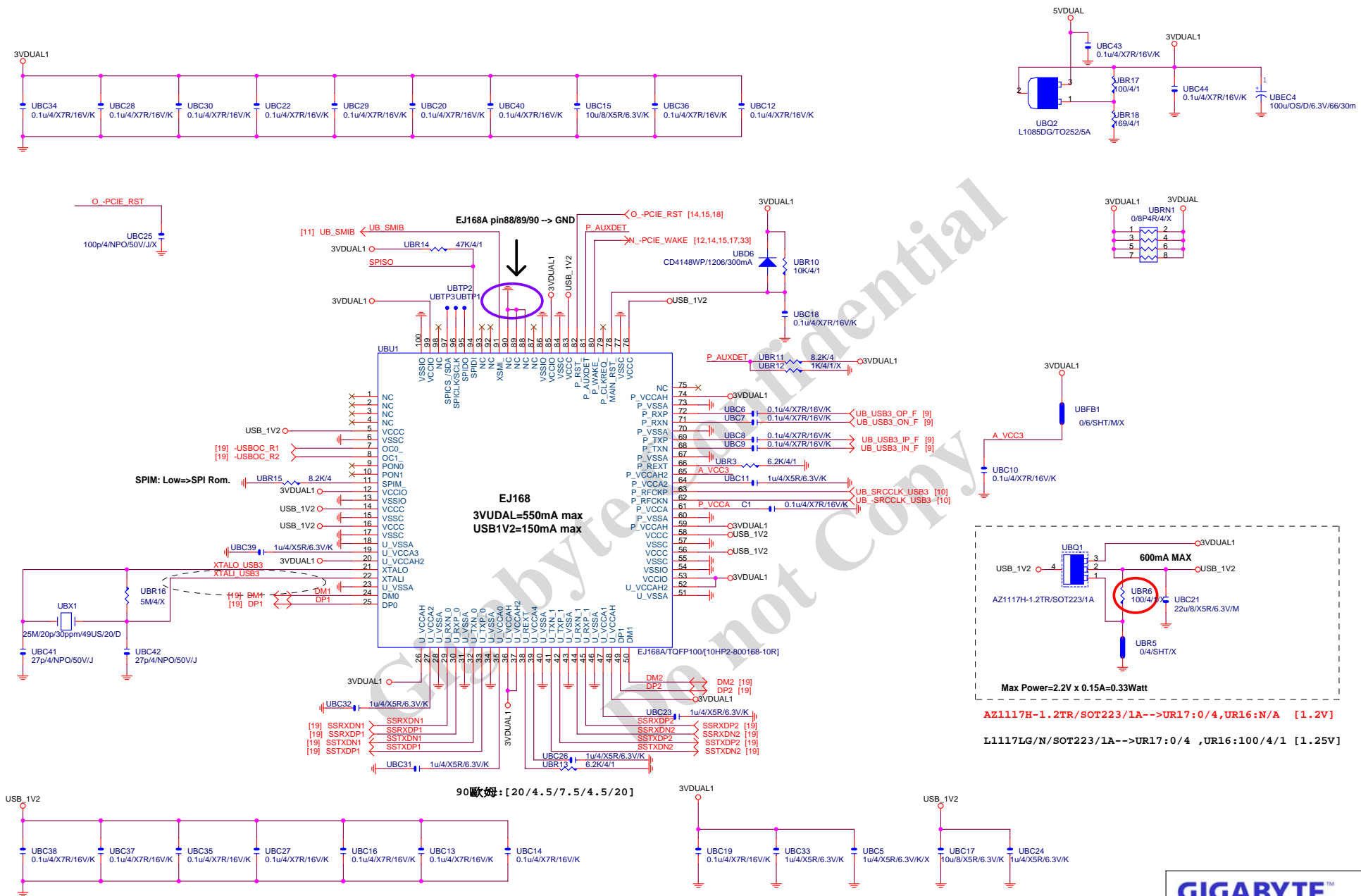


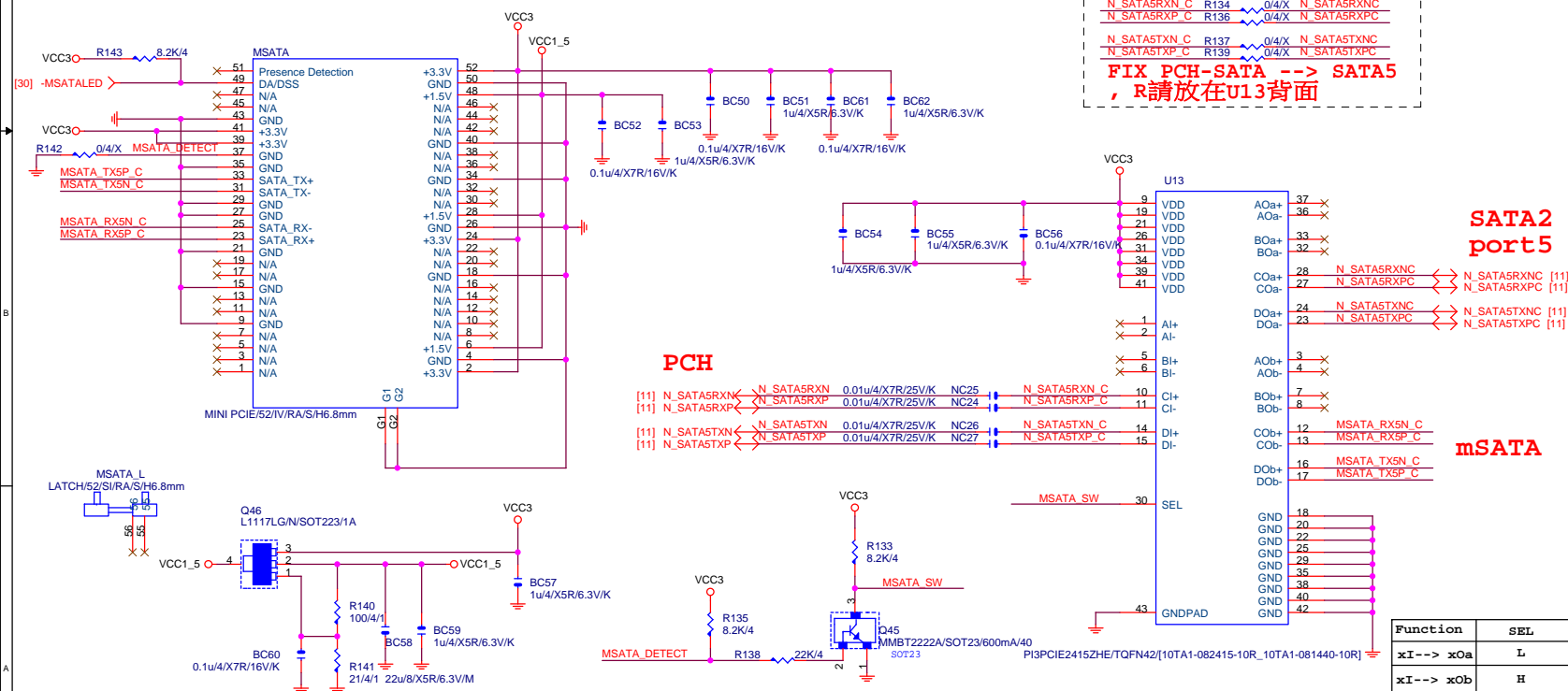
Figure 10: Close LAN chip. This diagram shows three identical circuit blocks connected to a common 3.3V supply. Each block contains a LAN chip (LA MD1+, LA MD2+, LA MD3+) and a LAN controller (LA MD1, LA MD2, LA MD3). The chips are connected to the 3.3V supply via a 10k resistor. The controllers are connected to the chips via a 10k resistor. The controllers are also connected to a common ground via a 10k resistor. The controllers are connected to a common ground via a 10k resistor. The controllers are connected to a common ground via a 10k resistor.

100歐姆:[20/4/8/4/20]

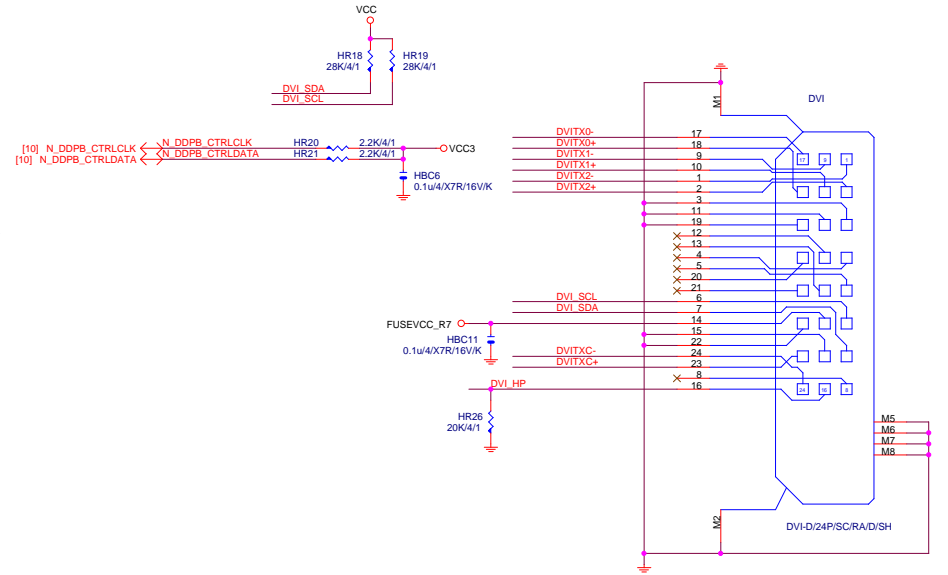
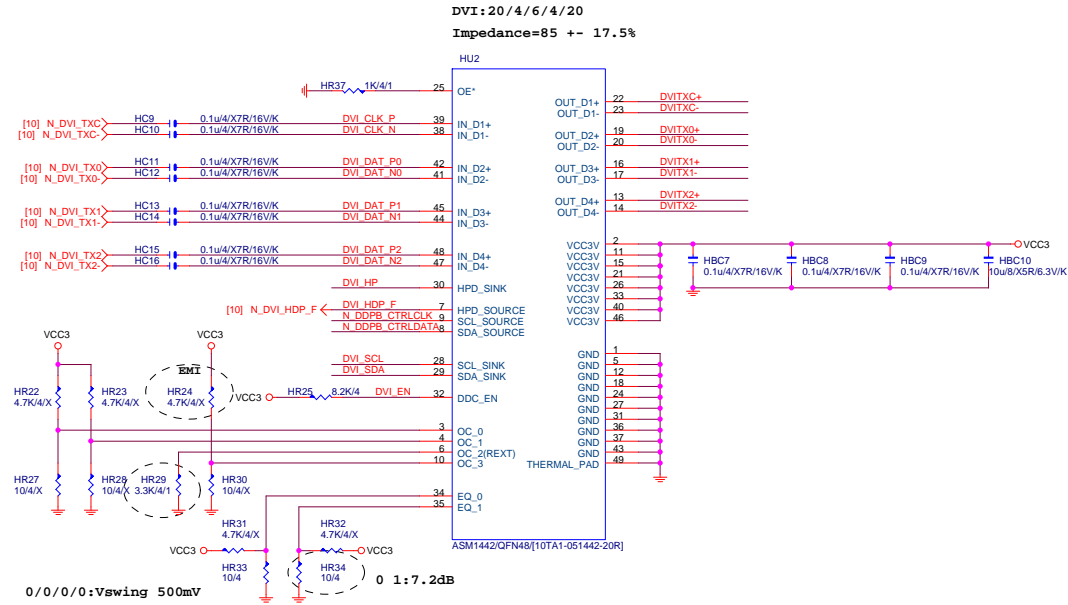




GIGABYTE™		
Title		
E-TRON EJ168		
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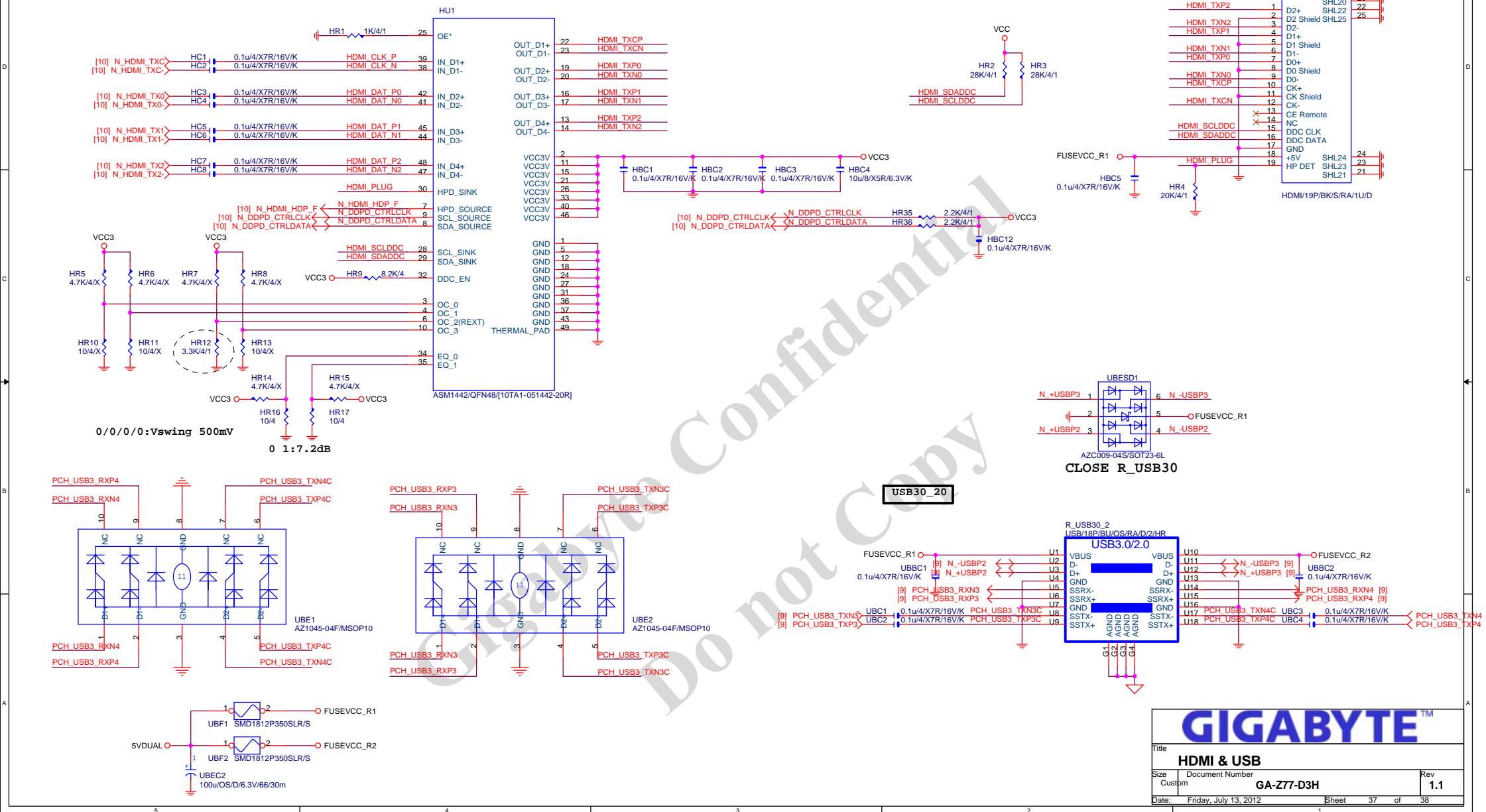


N_SATA5RXN C R134 0/4/X N_SATA5RXNC
 N_SATA5RXP C R136 0/4/X N_SATA5RXPNC
 N_SATA5TXN C R137 0/4/X N_SATA5TXNC
 N_SATA5TXP C R139 0/4/X N_SATA5TXPC
FIX PCH-SATA --> SATA5
, R請放在U13背面



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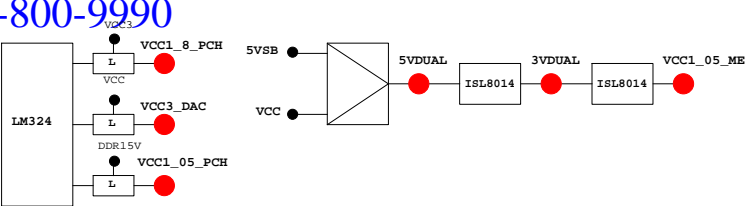
PCB GPIO LIST TABLE

PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI0	N/A
GP1/TACH1	MAIN		GPI01	N/A
GP2/PIRQE#	MAIN		GPI -PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI -PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI07	P/U 8.2K VCC3
GP8	STBY	H	GPI08	N/A
GP9/OC5#	STBY		NATIVE USB OC5#	N/A
GP10/OC6#	STBY		NATIVE USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI GPI012	N/A
GP13	STBY	L	GPI LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE USB OC7#	N/A
GP15	STBY	L	GPI GPI015(TLS Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI016	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI017	P/U 8.2K VCC3
GP18	MAIN		GPI Mobile Only	N/A
GP19	MAIN		GPI019	P/U 8.2K VCC3
GP20	MAIN		GPI020	P/U 8.2K VCC3
GP21	MAIN		GPI021	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI022	P/U 8.2K VCC3
GP23	MAIN		GPI023	N/A
GP24	STBY	L	GPI SKTOCC#	N/A
GP25	STBY		Mobile Only	N/A
GP26	STBY		Mobile Only	N/A
GP27	STBY	H	GPO GPI027	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO PWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI029	N/A
GP30	STBY	H-Z	GPI Mobile Only	N/A
GP31	STBY	H-Z	GPI Mobile Only	N/A
GP32	MAIN	H	GPO N/A	N/A
GP33	MAIN	H	GPO N/A	N/A
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO -ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI N/A	N/A
GP37	MAIN		GPI N/A	N/A
GP38	MAIN	H-Z	GPI PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI039	P/U 8.2K VCC3
GP40	STBY		NATIVE USB OC1#	N/A
GP41	STBY		NATIVE USB OC2#	N/A
GP42	STBY		NATIVE USB OC3#	N/A
GP43	STBY		NATIVE USB OC4#	N/A
GP44	STBY	L	NATIVE GPI044	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE GPI045	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE GPI046	P/U 8.2K 3VDUAL
GP47	STBY		Mobile Only	N/A
GP48	MAIN	H-Z	IN GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE -GNT1	N/A
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE -GNT2	N/A
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE -GNT3	N/A
GP56	STBY		NATIVE Mobile Only	N/A
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE -SUSTAT	N/A
GP62	STBY	L	NATIVE SUSCLK	N/A
GP63	STBY	L	NATIVE GPI063	N/A
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		Mobile Only	N/A
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL

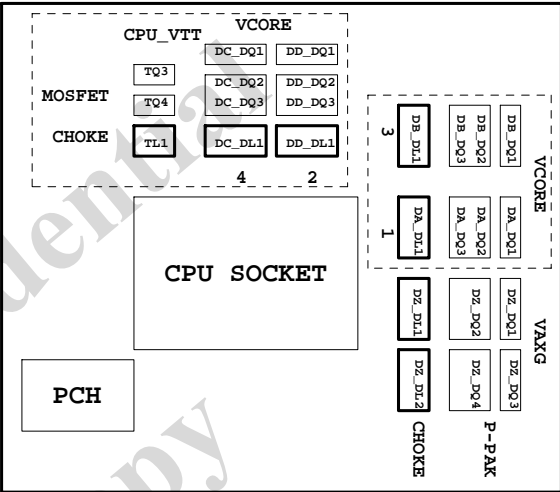
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VBSBW#/GP40	CS1_F0	BSEL166_1
SUSC#/GP53	CS1_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	2V PIN	FST_2X8
INIT#/GP85/SMB_D_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMB_D_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VID04/GP26/SCOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

Z77-D3H :
PCH :
12SP2-S05511-01R/02R/03R
MOSFET :
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
File	TABLE LIST		
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